Samsung
ARTIK™

10

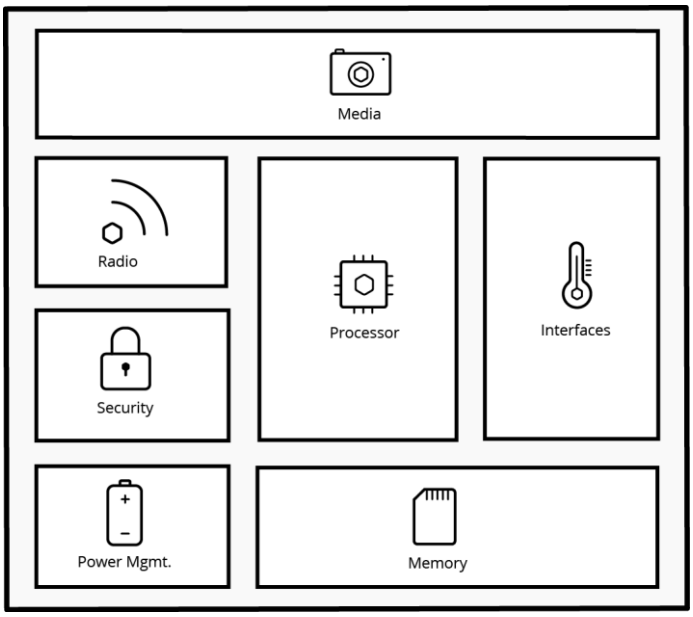
1020 Data Sheet

ARTIK 1020 Module Front View

Samsung's ARTIK™ 1020 Module is the world's highest performance Internet-of-Things (IoT) module. It is based on an octa-core architecture, containing quad ARM® Cortex®-A15 and ARM® quad Cortex®-A7 cores, DRAM and flash memory, camera and display interfaces, a full complement of digital I/O and analog inputs, and world class connectivity with IEEE802.11a/b/g/n/ac, Bluetooth® 4.1 + LE and a ZigBee® radio inside a package that is just 29x39x1.3mm.

The scalable processing power of the ARTIK 1020 Module makes it ideally suited for video and image processing tasks like autonomous vehicle navigation, intensive 3D graphics or large immersive displays.

Alternatively, the small size of the ARTIK 1020 Module enables servicing application domains with a high local computation requirement, like model-based robotic control, virtual reality or image processing. The hardware based Secure Element works with the ARM® TrustZone® and Trustonic's Trusted Execution Environment (TEE) to provide "bank level" security end-to-end.



ARTIK 1020 Module Block Diagram

Processor	
CPU	Quad core ARM® Cortex® A15@1.5GHz, Quad core Cortex® A7@1.3GHz
GPU	Mali™-T628 MP6 core
Media	
Camera I/F	1x 2-Lane MIPI CSI up to 3MP@30fps 1x 4-lane MIPI CSI up to 16MP@30fps (Supports YUV and MJPEG)
Display	4-lane MIPI DSI up to FHD 1920x1200@24bpp simultaneous HDMI 1920x1080@60fps
Audio	1x channel PCM and 2-channel I²S audio interface, supporting 5.1 channel audio
Memory	
DRAM	2GB LPDDR3
FLASH	16GB eMMC
Security	
Secure Element	Secure point to point authentication and data transfer
Trusted Execution Environment	Trustonic TEE (NDA required)
Radio	
WLAN	IEEE802.11a/b/g/n/ac
Bluetooth	4.1 + LE
IEEE802.15.4	ZigBee
Power Management	
PMIC	Provides all power of the ARTIK 1020 module using on board bucks and LDOs
Interfaces	
Analog and Digital I/O	GPIO, Analog Input, UART, I²C, I²S, SPI, USB 2.0, USB 3.0, SDIO, JTAG

Table of Contents

List of Figures

List of Tables

VERSION HISTORY

Revision	Date	Description	Maturity
1.10	October 19, 2016	ARTIK 1020 Module Data Sheet	Release

ARTIK 1020 Module Block Diagram

Figure 1 shows the functional block diagram of the ARTIK 1020 Module. It consists of a quad-core ARM® Cortex®-A15 with a quad-core A7 application processor with 2GB SDRAM and 16GB eMMC Flash, PMIC, Secure Element, Wi-Fi/BT chipset, ZigBee chipset, RF connectors and socket-type connectors.

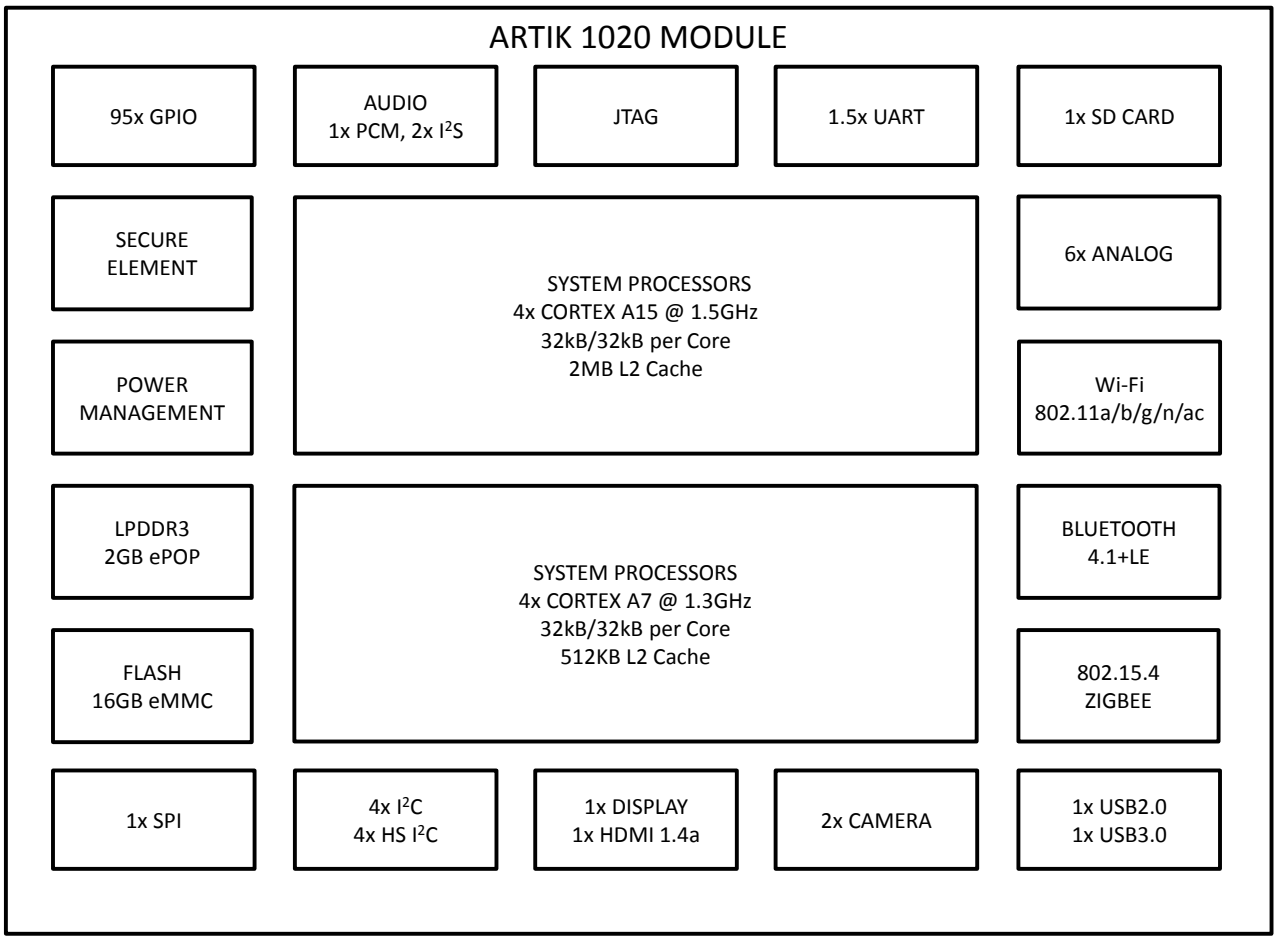


Figure 1. ARTIK 1020 Module Functional Block Diagram

The top side is populated with the ARM® application processor, SE, ZigBee, Wi-Fi/BT combo chipset and RF connectors for Wi-Fi/BT and ZigBee antennas. The bottom side is populated with the PMIC, Memory chipset and Secure Element, two main connectors for function connection to main set and one debug connector for debug interface connection.

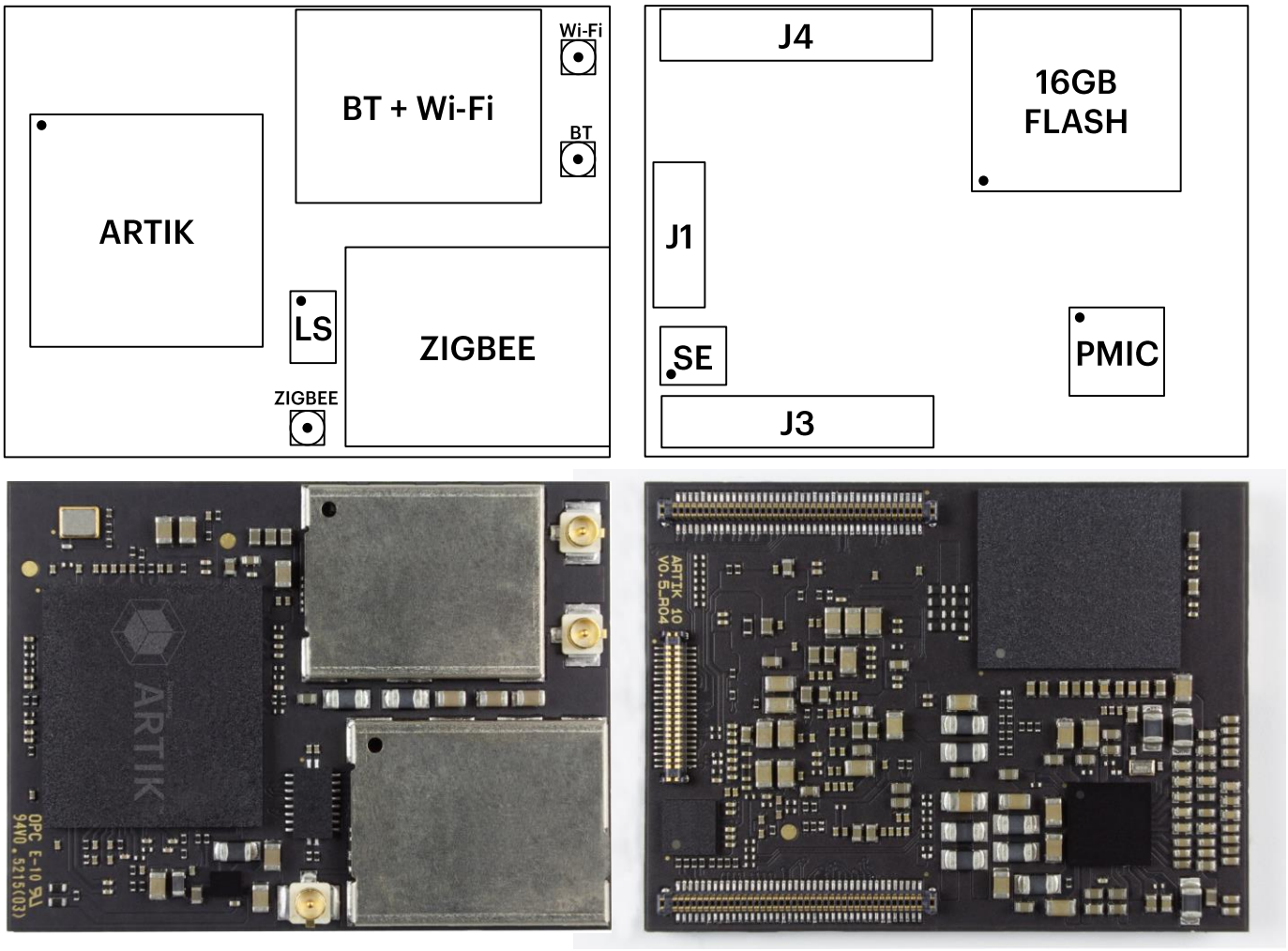


Figure 2. ARTIK 1020 Module – Top View / Bottom View

ARTIK 1020 Module Flash

The ARTIK 1020 Module carries an embedded 16GB Multi Media Card system that is version 5.0 compatible. The most important hardware features of the flash system are:

- Support for eMMC 5.0.
- Backward compatible with older eMMC specifications
- Support for variable databus width 1, 4 and 8 bits
- MMC I/F clock frequency 0-200MHz
- MMC I/F boot frequency 0-52MHz

For more information on KLMAG2GEAC-B002 contact a sales representative from Samsung Semiconductor, Inc.

ARTIK 1020 Module ZigBee

The ARTIK 1020 Module carries a fully integrated ZigBee unit called the Ember® EM3587. It integrates a 2.4 GHz, IEEE 802.15.4-2003-compliant transceiver, 32-bit ARM Cortex-M3 microprocessor, flash and RAM memory, and peripherals. The most important hardware features of the ZigBee module are:

- Complete system on chip using 32-bit ARM Cortex-M3 processor
- Low power consumption:
  - RX current typical 27mA
  - TX current typical 31mA
  - Deep sleep current ≤ 1.25µA
- RF performance:
  - Normal mode link budget up to 110dB
  - RX sensitivity up to 102dBm
- Robust Wi-Fi and Bluetooth coexistence
- Single voltage operation

For more information on EM3587 contact a sales representative from Silicon Laboratories, Inc.

ARTIK 1020 Module ZigBee Front End

The ARTIK 1020 Module carries a fully integrated RF Front-End Module (FEM) designed specifically for ZigBee Smart Energy IoT environments. The device provides integrated and fully matched input baluns, an integrated inter-stage matching and harmonic filter, and digital controls compatible with 1.6 to 3.6V CMOS levels. The RF blocks of the SE2432L support a wide range supply voltage tailored toward battery operated environments. The most important hardware features of the ZigBee front-end are:

- Integrated Power Amplifier up to 24dBm
- Integrated Low Noise Amplifier with programmable bypass
- Integrated antenna switching, with transmit and receive diversity function
- Low NF 2dB typical
- Differential transmit/receive interface with integrated baluns
- Fast switch on/off time ≤ 800ns
- Sleep mode current ≤ 0.05µA

For more information on SE2432L contact a sales representative from Skyworks Solutions, Inc.

ARTIK 1020 Module PMIC

The ARTIK 1020 Module has a fully integrated PMIC containing 10 bucks and 38 LDO's. This unit provides all power requirements for the ARTIK 1020 Module in one compact form factor. The 38 LDO regulators do have 31 PMOS LDOs
and 7NMOS LDOs. LDO28 is available on the debug connector.

For more information on S2MPS11B02 contact a sales representative from Samsung Semiconductor, Inc.

ARTIK 1020 Module Wi-Fi/Bluetooth

The ARTIK 1020 Module has a fully integrated MIMO combo BCM4354 for IEEE 802.11 a/b/g/n/ac wireless LAN with Bluetooth 4.0+LE and FM. The most important hardware features of the Wireless LAN Bluetooth combo module are:

- WLAN 802.11ac compliant:
  - Single stream spatial multiplexing up to 433Mbps
  - Support for 20, 40 and 80 MHz channels with optional SGI (256 QAM modulation)
- WLAN 802.11 a/b/g/n/ac compliant
- Bluetooth 4.0+LE
- 2G and 5G MIMO support
- FM Receiver 65MHz-108MHz bands

For more information on BCM4354 contact a sales representative from Broadcom Ltd.

ARTIK 1020 Module Secure Element

The ARTIK 1020 Module has a dedicated secure element to assure end to end authentication and communication between nodes in an IoT setting. The most important hardware features of the secure element are:

- Dedicated secure CPU SC300
- Crypto Accelerator
  - Hardware based AES/DES/3DES
  - TORNADO-E
  - 5KB crypto RAM
- Crypto co-processor
  - Modular exponential accelerator
  - RSA 4128bits/ECC 544 bits
- Data security
  - Abnormal condition detectors for: reset, interrupt, voltage, temperature, laser exposure, shield removal
  - Random Wait Generator, Random Current Generator
  - Secure optimized layout
  - Dynamic bus encryption
- Embedded tamper free memory
  - 1.5MB flash (program and data)
  - 32KB MASK ROM
  - 48KB Static RAM
  - 5KB Crypto RAM
  - Memory Protection Unit with 4GB addressable space
  - Secure flash write operation with fast page (0.5ms) and sector erase (4ms)
  - 500K erase/write cycles/s
- Serial interfaces:
  - I^2C/SPI/UART (ISO 7816)

- A guaranteed 25 years data retention at room temperature

For more information on S3FV5RP contact a sales representative from Samsung Semiconductor, Inc.

ARTIK 1020 Module Secure JTAG

Our secure JTAG core that is part of the ARTIK 1020 Module provides debug capabilities for the developer. The secure JTAG core authenticates the legal user and in addition it provides an access level that the legal user can operate under. The main features of the secure JTAG core are:

- Dedicated authentication process through password
- Dedicated Hash engine (SHA-1) with hash sequencer
- Two access levels “access-on” and “access-off”
- Industry standard JTAG capabilities

ARTIK 1020 Module Processor System

The processor system that resides on the ARTIK 1020 Module is a system-on-a-chip (SoC) based on a 32-bit RISC processor. Designed using the 28nm low power process the processor system provides superior performance using a quad core Cortex®-A15 and a quad core Cortex®-A7 CPU. The processor system contains WQXGA display capability, 3D graphics hardware, image signal processor hardware and a variety of high-speed interfaces such as eMMC5.0, and USB 3.0.

The ARTIK 1020 Module contains the quad core Cortex®-A15, which has a 40% increase in performance over the Cortex®-A9. It also incorporates a quad core Cortex®-A7 which enables energy efficient computing for less intensive tasks. The ARTIK 1020 Module allows for 14.9GB/s memory bandwidth for heavy traffic operations such as 1080p video en/decoding, 3D graphics display and high resolution image signal processing up to WQXGA resolutions.

The application processor supports dynamic virtual address mapping aiding software engineers to fully utilize the memory resources. The ARTIK 1020 Module 3D core's universal scalable shader engine supports the feature sets in Microsoft VS5.0 and PS5.0. The ARTIK 1020 Module supports Panel-Self-Refresh (PSR) to make a low power system which is important in an IoT environment. The native dual display, in particular, supports WQXGA resolution for the main LCD display and 1080p@60fps HDTV display through HDMI. The key features of the ARTIK 1020 Module are:

- Quad core ARM® Cortex®-A15 with NEON, 32 KB I$/32 KB D$ and 2MB L2 Cache
- Quad core ARM® Cortex®-A7, 32KB I$/32KB D$ and 512KB L2 Cache
- 128-bit Multi-layer Network-on-Chip (NoC) architecture
- Cache Coherent Interface (CCI) among Cortex®-A15 and Cortex®-A7, G2D, G3D and SSS
- Memory Subsystem:
  - 2-ports 32-bit up to 933 MHz LPDDR3/DDR3 Interfaces
  - 2-ports 32-bit up to 533 MHz LPDDR2 Interfaces
- 3D and 2D graphics hardware
- 1x port with 4-lanes MIPI DSI display interface for LCD, supporting up to FHD 1920x1200@24bpp RGB
- 1x HDMI 1.4a interface with on-chip PHY
- 1x port with 4-lanes MIPI CSI2 camera interface
- 1x port with 2-lanes MIPI CSI2 camera interface
- 1x channel USB 3.0 Host or Device (with USB2.0 backward compatibility), supporting SS (5 Gbps) with on-chip PHY
- 1x channel USB 2.0 Host, supporting LS/FS/HS (1.5 Mbps/12 Mbps/480 Mbps) with on-chip PHY
- 1x channel USB2.0 Device
- 1x channel 4-bit SD 3.0
- 1.5x channel high-speed UART (up to 3 Mbps data rate for Bluetooth 2.1 EDR and IrDA 1.0 SIR)

- 1x channel SPI
- 1x channel PCM and 2-channel I²S audio interface, supporting 5.1 channel audio
- 4x channel HS-I²C (up to 3.4 Mbps) for a variety of sensors (such as ambient light sensor, proximity sensor) and PMIC
- 4x channel I²C interface supporting (up to 400 kbps) for HDMI, general-purpose multi-master and ISP
- Security subsystem supporting hardware crypto accelerators, ARM® TrustZone® and TZASC
- 24x channel DMA Controller (8-channel MDMA, 8x2 channel PDMA)
- 87x Configurable Type A GPIOs and 8x Type B GPIOs
- Real time clock, PLLs, timer with PWM, MCT (Multi-Core Timer), and Watchdog timer

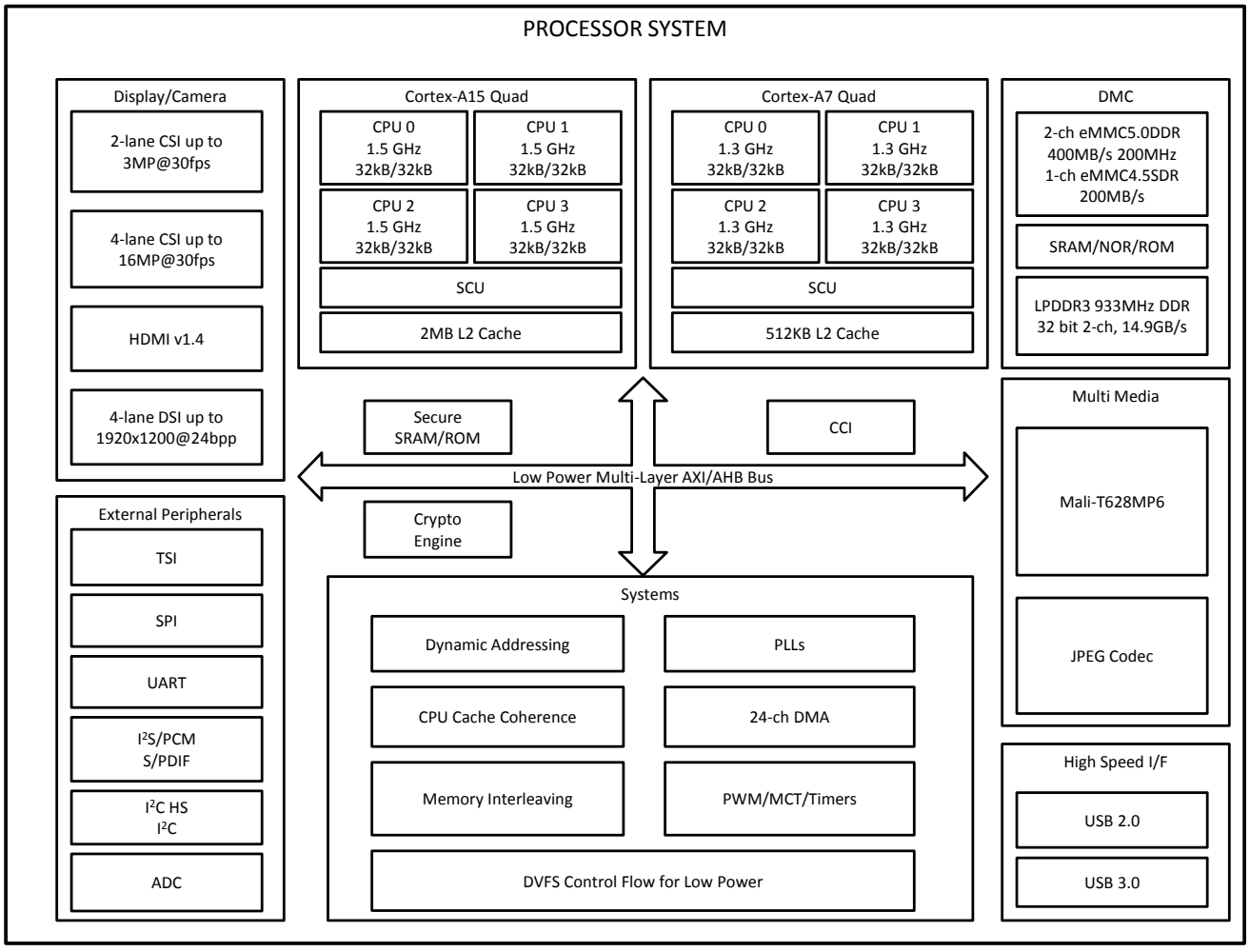


Figure 3. Processor System Block Schematic

Camera ISP

The processor system provides two main camera input channels (1x 4-channels, 1x 2-channels) that can process data up to 1.5 Gbps per channel using a MIPI CSI interface. The key features of the camera sub-system are:

- CAMIF (FIMC-LITE)
- Fully interactive mobile camera interface
- Input data through parallel I/F like ITU R BT-601 standard and MIPI (CSI) Slave I/F
- Consists of one input local path, output local port and output DMA port
- Supports input format of RAW8/10/12/14-bit+YUV422 8bit, MJPEG
- Supports MIPI VCI (virtual channel interleaving) up to 3 channels (single sensor). In dual sensor mode, 2-channel VCI + 1-channel
- 3 CAMIFs for dual sensor operation

HDMI v1.4

The ARTIK 1020 Module provides one HDMIv1.4 (High Definition Multimedia Interface) compliant interface. The key features of the HDMIv1.4 sub-system are:

- HDMI 1.4 with HDCP 1.4
- Support for video formats:
  - 480p@59.94Hz/60Hz, 576p@50Hz
  - 800x600@50Hz/60Hz
  - 720p@50Hz/59.94Hz/60Hz
  - 1280x800@60Hz
  - 1440x480i@60Hz
  - 1440x576i@50Hz
  - 1080i@50Hz/59.94Hz/60Hz
  - 1080p@50Hz/59.94Hz/60Hz
- Support for color formats:
  - RGB888/YCbCr444(YUV444)
  - 8-bit precision per color only
- Support for CEC function
- Includes an integrated high-bandwidth Digital Content Protection (HDCP) encryption engine for audio/video content protection

LCD Display

The ARTIK 1020 Module provides an LCD display capability using 1x MIPI interface that is compliant with the MIPI DSI standard specification V1.01. The key features of the LCD display sub-system are:

- Maximum resolution ranges up to FHD (1920x1200@24bpp)
- Supports 1, 2, 3, or 4 data lanes
- Supports pixel format: 16bpp, 18bpp packed, 18bpp loosely packed (3 byte format), and 24bpp
- Supported interfaces are:
  - Protocol-to-PHY Interface (PPI) in 1.0 Gbps/1.5Gbps MIPI D-PHY
  - RGB Interface for video image input from display controller
  - S-I80 (Synchronous I80) interface for Command Mode Image input from display controller
  - PMS control interface for PLL to configure byte clock frequency
  - Pre-scaler to generate escape clock from byte clock
  - Stereoscopic 3D, proprietary 3D, MIC input

SPI

The ARTIK 1020 Module provides 1x Serial Peripheral Interface (SPI) that transfers serial data. SPI support includes
8-bit/16-bit/32-bit shift registers to transmit and receive data. During a SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). Our SPI implementation adheres to the protocols described
by National Semiconductor, Microwire and Motorola's Serial Peripheral Interface. The key features of the SPI sub-system are:

- Support for full duplex
- 8-bit/16-bit/32-bit shift register for Tx and Rx
- 8-bit/16-bit/32-bit bus interface
- Complies with the SPI protocol described by National Semiconductor, Microwire and Motorola
- Support for 2 independent 32-bit wide transmit and receive FIFOs:
  - Depth 64 in SPI port 0 and depth 16 in SPI port 1 and 2
  - Depth 64 in ISP-SPI port 0 and 1
- Supports for master mode and slave mode
- Supports for receive-without-transmit operation
- Support Tx/Rx up to 50MHz

ADC

The ARTIK 1020 Module provides 6 channels of ADC input that are connected through a multiplexer to 1x12-bit ADC.
The key features of the ADC are:

- Up to 12-bit resolution per channel
- Conversion rate 30kSamples/s-600kSamples/s with a 600kHz-12MHz clock
- Programmable conversion mode (1, 2, 4, 8, 16, 32 or 64 times conversion)

UART

The ARTIK 1020 Module provides 1.5x (1x4-pin, 1x2-pin) independent UART channels and dedicated ISP UART channel.
The key features of the UART sub-system are:

- Both DMA and interrupt based mode of operation supported
- All independent channels support IrDA 1.0
- Each UART channel contains two FIFOs to receive and transmit data:
  - 256 bytes in ch0
  - 64 bytes in ch1
  - 64 bytes in ISP-UART ch0
  - 16 bytes in ch2 and ch3
- Each UART channel contains:
  - Programmable baud-rates
  - One or two stop bit insertion
  - 5-bit, 6-bit, 7-bit, or 8-bit data width
  - Parity checking

I²S

The ARTIK 1020 Module provides 2x, 3 line Inter-IC Sound (I^2S) channels. The I^2S interface is one of the most popular digital audio interfaces. The I^2S bus handles audio data and other signals such as sub-coding and control. It is possible to transmit data between two I^2S buses. To minimize the number of pins required and to keep wiring simple, a 3-line serial bus is used. The key features of the I^2S sub-system are:

- Mixes up to 2 sound sources
- Drives primary sound source up to 5.1ch using I^2S-bus with external DMA-based operation
- Supports secondary sound source up to stereo with internal or external DMA
- Supports I^2S TDM mode: 1-8 slots (7.1 channels) for transmission (Tx) and 1-2 slots (2 channels) for reception (Rx)
- Supports serial data transfer of 8/16/24-bit per channel
- Supports I^2S, MSB-justified, and LSB-justified data formats
- Supports both master and slave modes
- Supports auxiliary clock out for codec chip

PCM

The ARTIK 1020 Module provides 1x PCM channel. The PCM audio interface provides a bi-directional serial interface
to an external codec. The key features of the PCM sub-system are:

- 16-bit PCM and three ports audio interface
- Supports only Master mode
- All PCM serial timings and strobes are extracted from one master clock
- Supports 1x input (16-bit x 32depth) and 1x output (16-bit x 32 depth) FIFO to buffer data
- DMA interface for Tx or Rx, or both

GPIO

The ARTIK 5 Module provides a GPIO system to allow for a wide variety of use cases to be supported. The key features of the GPIO system are:

- Control for up to 88 external interrupts
  - Falling edge triggered

  - Rising edge triggered
  - Both edge triggered
- Control for up to 25 wake-up interrupts
  - Falling edge triggered
  - Rising edge triggered
  - Both edge triggered
- Control for up to 95 General Purpose IOs
- Controls a variety of pin states in sleep mode

I²C

The ARTIK 1020 Module provides 4x High Speed (HS) I²C channels, in addition it also provides 4x I²C channels. The key features of the I²C module are:

- 4x HS I²C channels up to 3.4Mb/s
- 4x I²C channels up to 400kb/s:
  - Supporting master and slave mode
  - 7-bit addressing mode only
  - Supports serial, 8-bit oriented and bi-directional data transfer
  - Supports up to 100 kb/s in the standard mode
  - Supports up to 400 kb/s in the fast mode
  - Supports master transmit, master receive, slave transmit, and slave receive operation
  - Supports both interrupt and polling events

USB

The ARTIK 1020 Module provides 1x USB2.0 host interface and 1x USB3.0 interface. The key features of the USB2.0 module are:

- In compliance with the Enhanced Host Controller Interface (EHCI) specification, version 1.1 and the Open Host Controller Interface (OHCI) specification, version 1.0a
- In compliance with the USB 2.0 specification
- In compliance with the both the legacy UTMI revision 1.05 and the UTMI+ Level3 revision 1.0
- Supports high-speed, full speed and low speed transfers
- Supports power management features, such as: Suspend/resume functionality, including remote wakeup
- Over-current protection

The key features of the USB3.0 module are:

- In compliance with USB device 3.0 and USB device 2.0
- In compliance with USB host 3.0 and USB host 2.0
- Supports USB device 3.0 interface and USB device 2.0 interface
- Supports USB host 3.0 interface and USB host 2.0 interface
- Supports full-speed (12 Mbps) and high-speed (480 Mbps) modes with USB Device 2.0 interface
- Supports super-speed (5 Gbps) mode with USB device 3.0 interface
- Supports one physical USB port meaning the physical port can be used with either USB 3.0 or USB 2.0
- Supports on-chip USB PHY transceiver
- Supports flexible endpoint configuration
- Supports up to 16 bi-directional endpoints, including control endpoint 0

Mali™-T600 Series

The ARTIK 1020 Module provides 1x instance of the Mali™-T600 GPU series from ARM®. The Mali™-T600 series adds graphics capabilities to the ARTIK 1020 Module. The key features of the Mali™-T600 module are:

- Double precision image processing with FP64 and anti-aliasing
- Coherency aware memory architecture
- Support for EGL 1.4

DMC

The ARTIK 1020 Module provides a Dynamic Memory Controller (DMC) that supports the following memory interfaces:

- 2x channel eMMC5.0 DDR@400MB/s
- 1x channel eMMC4.5 SDR@200MB/s
- SRAM/NOR/ROM interface
- LP-DDR3@933MHz interface
- 2x channel 32-bit DDR3@14.9GB/s

Quad Cortex®-A15 plus Quad Cortex®-A7

The ARTIK 1020 Module provides eight CPU cores which consist of ARM Cortex-A15 quad core processors and ARM Cortex-A7 quad core processors. The Cortex-A15 cores are targeted toward high performance functions while the Cortex-A7 cores are optimized for power efficient computations. For easier and faster CPU core switching, the ARTIK 1020 Module supports a cache coherency interconnect (CCI) bus with L2 cache snooping capability. This hardware automatically assures cache coherency between the 2x L2 caches, so manually synchronizing contents is not needed. The ARM Cortex-A7/A15 octa-core has the following common features:

- Common ARMv7-A Cortex architecture
- Advanced SIMD version 2 with architecture extensions for integer and floating-point vector operations
- Vector floating-point version 4 architecture extensions for floating-point computation that is fully compliant with the IEEE 754 standard
- TrustZone® security technology for ensuring reliable implementation
- Virtualization extensions for the development of virtualized systems that enables the switching of guest operating systems
- Large Physical Address Extension (LPAE) for address translation of up to 40 bits physical address space
- AMBA 4 Cache Coherent Interconnect (CCI)
- ARM NEON™ with 128-bit SIMD
- Multiprocessing extensions for multiprocessing functionality

The ARM Cortex-A15 has the following specific features:

- 3.5 DMIPS per core
- 32KB/32KB I$/D$ and 2MB L2 cache
- 1 TB physical addressing space
- Full hardware virtualization
- ECC and parity protection for all SRAMs
- Advanced power management
- Improved single-thread and MP performance

The ARM Cortex-A7 has the following specific features:

- 1.86 DMIPS per core
- 32KB/32KB I$/D$ cache and 512KB L2 cache
- Rapid switch companion to Cortex-A15

Associated with the eight CPU cores, the ARTIK 1020 Module provides a generic interrupt controller and multi-core timers for each CPU core. The interrupt controller and timer are always-alive even when the CPU cores are power gated. The key features of the generic interrupt controller are:

- Support for three interrupt types:
  - Software Generated Interrupt (SGI)
  - Private Peripheral Interrupt (PPI)
  - Shared Peripheral Interrupt (SPI)
- Programmable interrupts that:
  - Set the security state for an interrupt
  - Set the priority level of an interrupt
  - Enable or disable the interrupt
  - Inform the processors that receives an interrupt
- Enhanced security features

The key features of the multi-core timers are:

- Eight local timers, one for each CPU core containing:
  - A 32-bit counter that generates an interrupt when it reaches zero
  - Single-shot or auto-reload mode
  - Configurable starting value per timer
- A global timer:
  - With a 64-bit incrementing counter and an auto-incrementing feature
  - Accessible to all Cortex-A15/Cortex-A7 processors

ARTIK 1020 Module Connectors

The ARTIK 1020 Module utilizes 2x 80-position and 2x 40-position connectors providing support for GPIO, ADC, SPI, OM, USB, UART, PWM, ISP, I^{2}C, MIPI, HDMI and JTAG. Connector J3 and J4 indicated by AXT480124 are from Panasonic and have 80 pins with a 0.4mm pitch. Connector J1 and J9 indicated by AXT440124 are also from Panasonic and have 40 pins with a 0.4mm pitch. For additional information on both AXT480124 and AXT440124 please contact Panasonic.

In *Figure 4* a listing of all power/signal names that are assigned to physical pins of connector J3 and connector J4 are given. In *Table 1* and *Table 2* the functions and electrical limitations associated with physical behavior of the pins is described. Functionally Connector J3 carries the following interfaces: SPI, I^{2}C, ADC, USB3.0 CH0, I^{2}S/PCM, UART, GPIO and PWM. Functionally Connector J4 carries the following interfaces: ISP, I^{2}C, GPIO, PWM, USB HOST, USB3.0, MMC and MIPI. In general the Interrupts, GPIO and I^{2}C functionality that is present on the connector's might be support for the other interfaces present on the connector.

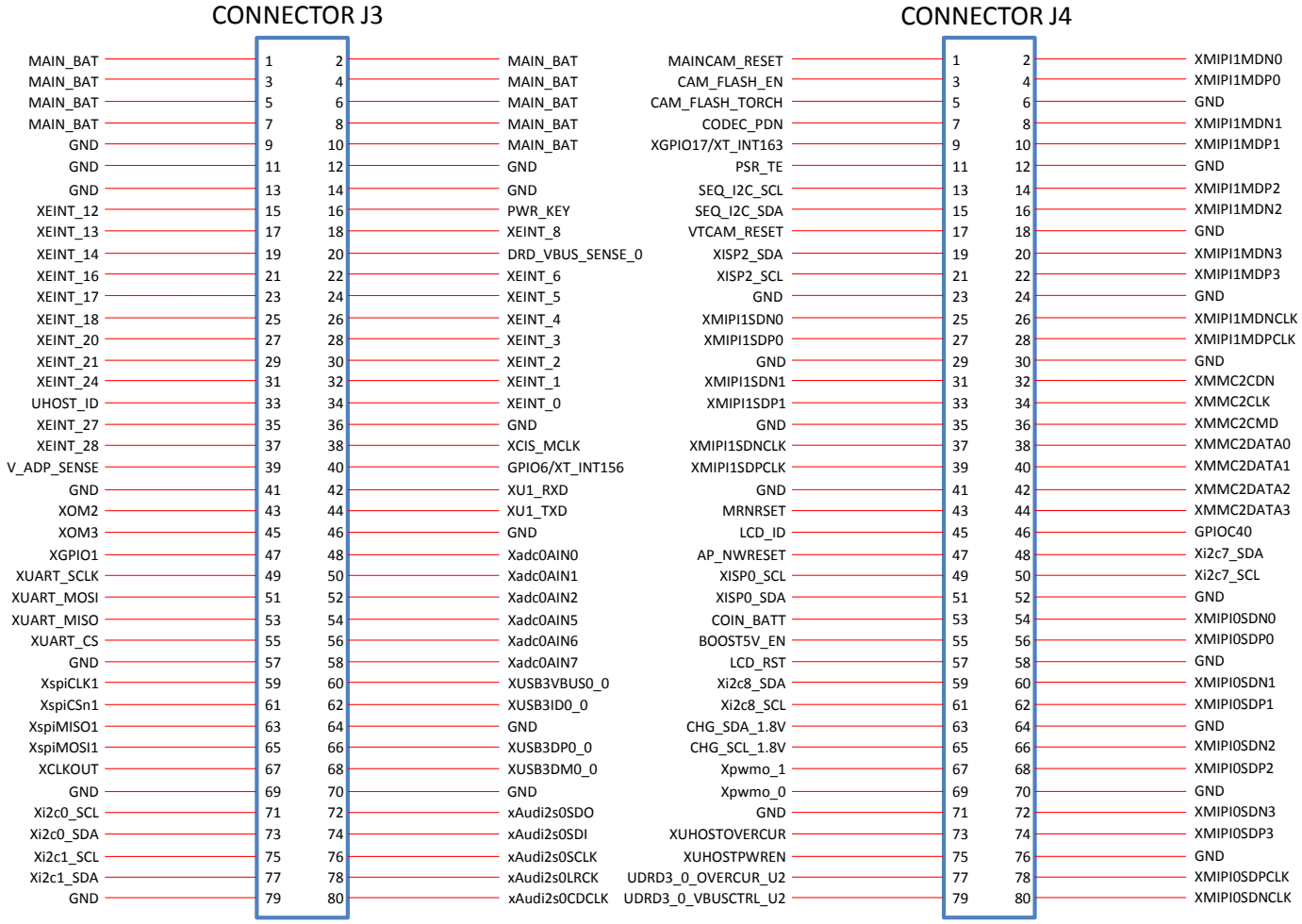


Figure 4. Connector J3, J4 Pin Layout

CONNECTOR J3

Table 1. Connector J3 Pin Description

Connector J3									
Conn#	Pin#	Name	I/O Type	Default	Voltage	DS [mA]	PUD*	Group	Function
J3	1	MAIN_BAT	NA		3V8	NA		BATTERY	Power source (3.8V)
J3	3	MAIN_BAT	NA		3V8	NA		BATTERY	Power source (3.8V)
J3	5	MAIN_BAT	NA		3V8	NA		BATTERY	Power source (3.8V)
J3	7	MAIN_BAT	NA		3V8	NA		BATTERY	Power source (3.8V)
J3	9	GND	NA		0V0	NA		GROUND	Ground
J3	11	GND	NA		0V0	NA		GROUND	Ground
J3	13	GND	NA		0V0	NA		GROUND	Ground
J3	15	XEINT_12	A	I	1V8	2	PDE	LCD	MIPI error detection
J3	17	XEINT_13	A	I	1V8	2	PDE	ARDUINO	GPIO
J3	19	XEINT_14	A	I	1V8	2	PDE	ARDUINO	GPIO
J3	21	XEINT_16	A	I	1V8	2	PDE	Wi-Fi/BT	GPIO
J3	23	XEINT_17	A	I	1V8	2	PDE	POWER/RESET	CHG_IRQ
J3	25	XEINT_18	A	I	1V8	2	PDE	UARTS	XUART_RST
J3	27	XEINT_20	A	I	1V8	2	PDE	UARTS	XUART_IRQ
J3	29	XEINT_21	A	O	1V8	2	PDE	LCD	TP_RST
J3	31	XEINT_24	A	I	1V8	2	PDE	LCD	TP_INT
J3	33	UHOST_ID	A	EXT_INT43[1]	1V8	2	PUDD	NA	UHOST_ID
J3	35	XEINT_27	A	I	1V8	2	PDE	AUDIO	JACK_DET
J3	37	XEINT_28	A	I	1V8	2	PDE	Wi-Fi/BT	LVDS_RST
J3	39	V_ADP_SENSE	A	I	1V8	2	PDE	POWER/RESET	V_ADP_SENSE
J3	41	GND	NA		0V0	NA		GROUND	Ground
J3	43	XOM2	PROCESSOR		1V8	NA		POWER/RESET	SDMMC_CH2 or eMMC44_CH0 boot
J3	45	XOM3	PROCESSOR		1V8	NA		POWER/RESET	SDMMC_CH2 or eMMC44_CH0 boot
J3	47	XGPIO1	A	I	1V8	2	PDE	CAMERA	Power down
J3	49	XUART_SCLK	A	I	1V8	2	PDE	UARTS	GENERIC UART SCLK
J3	51	XUART_MOSI	A	I	1V8	2	PDE	UARTS	GENERIC UART MOSI
J3	53	XUART_MISO	A	I	1V8	2	PDE	UARTS	GENERIC UART MISO
J3	55	XUART_CS	A	I	1V8	2	PDE	UARTS	GENERIC UART CS
J3	57	GND	NA		0V0	NA		GROUND	Ground
J3	59	XspiCLK1	A	I	1V8	2	PDE	Wi-Fi/BT/SIGFOX	SPI CLK
J3	61	XspiCSn1	A	I	1V8	2	PDE	SIGFOX	SPI CSn
J3	63	XspiMISO1	A	I	1V8	2	PDE	Wi-Fi/BT/SIGFOX	SPI MISO
J3	65	XspiMOSI1	A	I	1V8	2	PDE	Wi-Fi/BT/SIGFOX	SPI MOSI
J3	67	XCLKOUT	NA		1V8	NA		AUDIO	24MHz CDCLK
J3	69	GND	NA		0V0	NA		GROUND	Ground
J3	71	Xi2c0_SCL	A	I	1V8	2	PDE	POWER/RESET	SCL
J3	73	Xi2c0_SDA	A	I	1V8	2	PDE	POWER/RESET	SDC
J3	75	Xi2c1_SCL	A	I2C_1_SCL	1V8	2	PUE	Wi-Fi/BT/AUDIO	SCL for BT audio
J3	77	Xi2c1_SDA	A	I2C_1_SDA	1V8	2	PUE	Wi-Fi/BT/AUDIO	SDA for BT audio
J3	79	GND	NA		0V0	NA		GROUND	Ground
J3	2	MAIN_BAT	NA		3V8	NA		BATTERY	Power source (3.8V)
J3	4	MAIN_BAT	NA		3V8	NA		BATTERY	Power source (3.8V)

Connector J3									
Conn#	Pin#	Name	I/O Type	Default	Voltage	DS [mA]	PUD*	Group	Function
J3	6	MAIN_BAT	NA		3V8	NA		BATTERY	Power source (3.8V)
J3	8	MAIN_BAT	NA		3V8	NA		BATTERY	Power source (3.8V)
J3	10	MAIN_BAT	NA		3V8	NA		BATTERY	Power source (3.8V)
J3	12	GND	NA		0V0	NA		GROUND	Ground
J3	14	GND	NA		0V0	NA		GROUND	Ground
J3	16	PWR_KEY	PMIC		1V8	NA		POWER/RESET	power on, high active
J3	18	XEINT_8	A	I	1V8	2	PDE	ARDUINO	GPIO
J3	20	DRD_VBUS_SENSE_0	A	EXT_INT40[7]	1V8	2	PDE	USB3.0	DRD_VBUS_SENSE_0
J3	22	XEINT_6	A	I	1V8	2	PDE	ARDUINO	GPIO
J3	24	XEINT_5	A	I	1V8	2	PDE	ARDUINO	GPIO
J3	26	XEINT_4	A	I	1V8	2	PDE	ARDUINO	GPIO
J3	28	XEINT_3	A	I	1V8	2	PDE	ARDUINO	GPIO
J3	30	XEINT_2	A	I	1V8	2	PDE	ARDUINO	GPIO
J3	32	XEINT_1	A	I	1V8	2	PDE	ARDUINO	GPIO
J3	34	XEINT_0	A	I	1V8	2	PDE	ARDUINO	GPIO
J3	36	GND	NA		0V0	NA		GROUND	Ground
J3	38	XCIS_MCLK	A	I	1V8	2	PDE	CAMERA	MCLK
J3	40	GPIO6/XT_INT156	A	I	1V8	2	PDE	CAMERA	MCLK
J3	42	Xu1_RXD	A	UART_1_RXD	1V8	2	PUDD	ARDUINO	UART RXD
J3	44	Xu1_TXD	A	UART_1_TXD	1V8	2	PUDD	ARDUINO	UART TXD
J3	46	GND	NA		0V0	NA		GROUND	Ground
J3	48	Xadc0AIN0	Analog		1V8	NA		ARDUINO	ADC
J3	50	Xadc0AIN1	Analog		1V8	NA		ARDUINO	ADC
J3	52	Xadc0AIN2	Analog		1V8	NA		ARDUINO	ADC
J3	54	Xadc0AIN5	Analog		1V8	NA		ARDUINO	ADC
J3	56	Xadc0AIN6	Analog		1V8	NA		ARDUINO	ADC
J3	58	Xadc0AIN7	Analog		1V8	NA		ARDUINO	ADC
J3	60	XUSB3VBUS0_0	USB3.0		3V3	NA		USB3.0	USB3.0 DRD channel 0
J3	62	XUSB3ID0_0	A/USB3.0/ADC	EXT_INT43[5]	1V8	2	PUE	USB3.0	Identification USB3.0 DRD channel 0
J3	64	GND	NA		0V0	NA		GROUND	Ground
J3	66	XUSB3DP0_0	USB3.0		3V3	NA		USB3.0	USB2.0 backward compatible P channel in USB3.0
J3	68	XUSB3DM0_0	USB3.0		3V3	NA		USB3.0	USB2.0 backward compatible M channel in USB3.0
J3	70	GND	NA		0V0	NA		GROUND	Ground
J3	72	xAudi2s0SDO	A		1V8			Wi-Fi/BT/AUDIO	Audio SDO
J3	74	xAudi2s0SDI	A		1V8			Wi-Fi/BT/AUDIO	Audio SDI
J3	76	xAudi2s0SCLK	A		1V8			Wi-Fi/BT/AUDIO	Audio SCLK
J3	78	xAudi2s0LRCK	A		1V8			Wi-Fi/BT/AUDIO	Audio LRCK
J3	80	xAudi2s0CDCLK	A		1V8			Wi-Fi/BT/AUDIO	Audio DCLK

* The PUD variables have the following meaning:
PUDD = Power Up Down Disabled, PDE = Power Down Enabled, PUE = Power Up Enabled, R = Reserved.

CONNECTOR J4

Table 2. Connector J4 Pin Description

Connector J4									
Conn#	**Pin#**	**Name**	**I/O Type**	**Default**	**Voltage**	**DS [mA]**	**PUD***	**Group**	**Function**
J4	1	MAINCAM_RESET	A	I	1V8	2	PDE	CAMERA	Reset
J4	3	CAM_FLASH_EN	A	O	1V8	2	PDE	CAMERA	Flash
J4	5	CAM_FLASH_TORCH	A	O	1V8	2	PDE	CAMERA	Flash torch
J4	7	CODEC_PDN	A	O	1V8	2	PDE	Wi-Fi/BT/AUDIO	Codec Power Down
J4	9	XGPIO17/XT_INT163	A	I	1V8	2	PDE	SIGFOX	Low power control
J4	11	PSR_TE	A	I	1V8	2	PDE	ISP	Display sync
J4	13	SEQ_I2C_SCL	A	I	1V8	2	PDE	SPI	SCL
J4	15	SEQ_I2C_SDA	A	I	1V8	2	PDE	SPI	SDA
J4	17	VTCAM_RESET	A	I	1V8	2	PDE	CAMERA	Reset
J4	19	XISP2_SDA	A	I	1V8	2	PDE	CAMERA	SDA
J4	21	XISP2_SCL	A	I	1V8	2	PDE	CAMERA	SCL
J4	23	GND	NA		0V0	NA		GROUND	Ground
J4	25	XMIPI1SDN0	MIPI		1V0	NA		CAMERA	CSI1 SDN0 CHANNEL 0
J4	27	XMIPI1SDP0	MIPI		1V0	NA		CAMERA	CSI1 SDP0 CHANNEL 0
J4	29	GND	NA		0V0	NA		GROUND	Ground
J4	31	XMIPI1SDN1	MIPI		1V0	NA		CAMERA	CSI1 SDN1 CHANNEL 1
J4	33	XMIPI1SDP1	MIPI		1V0	NA		CAMERA	CSI1 SDP1 CHANNEL 1
J4	35	GND	NA		0V0	NA		GROUND	Ground
J4	37	XMIPI1SDNCLK	MIPI		1V0	NA		CAMERA	CSI1 SDNCLK
J4	39	XMIPI1SDPCLK	MIPI		1V0	NA		CAMERA	CSI1 SDPCLK
J4	41	GND	NA		0V0	NA		GROUND	Ground
J4	43	MRNRESET	PROCESSOR /PMIC		1V8	NA		POWER/RESET/ARDUINO/ SENSOR/ Wi-Fi/BT	PMIC resets Processor Subsystem
J4	45	LCD_ID	A	I	1V8	2	PDE	SIGFOX	Vsync
J4	47	AP_NWRESET	PROCESSOR	I	1V8	-	-	NA	Warm Reset
J4	49	XISP0_SCL	A	I	1V8	2	PDE	CAMERA	SCL
J4	51	XISP0_SDA	A	I	1V8	2	PDE	CAMERA	SDA
J4	53	COIN_BATT	NA	NA	3V3	-	-	NA	Coin Battery Power Supply
J4	55	BOOST5V_EN	A	O	1V8	2	PDE	USB3.0	USB3.0
J4	57	LCD_RST	A	O	1V8	2	PUE	LCD	Reset
J4	59	Xi2c8_SDA	A	I	1V8	2	PDE	LCD	SCL
J4	61	Xi2c8_SCL	A	I	1V8	2	PDE	LCD	SDA
J4	63	CHG_SDA_1.8V	A	I	1V8	2	PUE	POWER/RESET	Change I2C to 1V8 signaling
J4	65	CHG_SCL_1.8V	A	I	1V8	2	PUE	POWER/RESET	Change I2C to 1V8 signaling
J4	67	Xpwmo_1	A	I	1V8	2	PDE	ARDUINO	PWM On/Off control
J4	69	Xpwmo_0	A	I	1V8	2	PDE	ARDUINO	PWM On/Off control
J4	71	GND	NA		0V0	NA		GROUND	Ground
J4	73	XUHOSTOVERCUR	USB HOST		1V8	NA		NA	
J4	75	XUHOSTPWREN	USB HOST		1V8	NA		USB/ETHERNET	USB
J4	77	UDRD3_0_OVERCUR_U2	USB3.0		1V8	NA		USB3.0	Control for USB3.0 DRD channel 0
J4	79	UDRD3_0_VBUSCTRL_U2	USB3.0		1V8	NA		USB3.0	Control for USB3.0 DRD channel 0
J4	2	XMIPI1MDN0	MIPI		1V0	NA		LCD	DSI1 DN0 CHANNEL 0
J4	4	XMIPI1MDP0	MIPI		1V0	NA		LCD	DSI1 DP0 CHANNEL 0

Connector J4									
Conn#	Pin#	Name	I/O Type	Default	Voltage	DS [mA]	PUD*	Group	Function
J4	6	GND	NA		0V0	NA		GROUND	Ground
J4	8	XMIPI1MDN1	MIPI		1V0	NA		LCD	DSI1 DN1 CHANNEL 1
J4	10	XMIPI1MDP1	MIPI		1V0	NA		LCD	DSI1 DP1 CHANNEL 1
J4	12	GND	NA		0V0	NA		GROUND	Ground
J4	14	XMIPI1MDP2	MIPI		1V0	NA		LCD	DSI1 DP2 CHANNEL 2
J4	16	XMIPI1MDN2	MIPI		1V0	NA		LCD	DSI1 DN2 CHANNEL 2
J4	18	GND	NA		0V0	NA		GROUND	Ground
J4	20	XMIPI1MDN3	MIPI		1V0	NA		LCD	DSI1 DN3 CHANNEL 3
J4	22	XMIPI1MDP3	MIPI		1V0	NA		LCD	DSI1 DP3 CHANNEL 3
J4	24	GND	NA		0V0	NA		GROUND	Ground
J4	26	XMIPI1MDNCLK	MIPI		1V0	NA		LCD	DSI1 NCLK
J4	28	XMIPI1MDPCLK	MIPI		1V0	NA		LCD	DSI1 PCLK
J4	30	GND	NA		0V0	NA		GROUND	Ground
J4	32	XMMC2CDN	B		2V8	8	PUE	SD CARD	CDN card detect
J4	34	XMMC2CLK	B		2V8	8	PUDD	SD CARD	CLK
J4	36	XMMC2CMD	B		2V8	8	PUDD	SD CARD	CMD
J4	38	XMMC2DATA0	B		2V8	8	PUE	SD CARD	DATA0
J4	40	XMMC2DATA1	B		2V8	8	PUE	SD CARD	DATA1
J4	42	XMMC2DATA2	B		2V8	8	PUE	SD CARD	DATA2
J4	44	XMMC2DATA3	B		2V8	8	PUE	SD CARD	DATA3
J4	46	GPIOC40	B	I	2V8	2	PDE	POWEWR/RESET	GPIO
J4	48	Xi2c7_SDA	A	I	1V8	2	PDE	HDMI	SCL
J4	50	Xi2c7_SCL	A	I	1V8	2	PDE	HDMI	SDA
J4	52	GND	NA	-	0V0	NA		GROUND	Ground
J4	54	XMIPI0SDN0	MIPI	-	1V0	NA		CAMERA	CSI0 DN0 CHANNEL 0
J4	56	XMIPI0SDP0	MIPI	-	1V0	NA		CAMERA	CSI0 DP0 CHANNEL 0
J4	58	GND	NA	-	0V0	NA		GROUND	Ground
J4	60	XMIPI0SDN1	MIPI	-	1V0	NA		CAMERA	CSI0 DN1 CHANNEL 1
J4	62	XMIPI0SDP1	MIPI	-	1V0	NA		CAMERA	CSI0 DP1 CHANNEL 1
J4	64	GND	NA	-	0V0	NA		GROUND	Ground
J4	66	XMIPI0SDN2	MIPI	-	1V0	NA		CAMERA	CSI0 DN2 CHANNEL 2
J4	68	XMIPI0SDP2	MIPI	-	1V0	NA		CAMERA	CSI0 DP2 CHANNEL 2
J4	70	GND	NA	-	0V0	NA		GROUND	Ground
J4	72	XMIPI0SDN3	MIPI	-	1V0	NA		CAMERA	CSI0 DN3 CHANNEL 3
J4	74	XMIPI0SDP3	MIPI	-	1V0	NA		CAMERA	CSI0 DP3 CHANNEL 3
J4	76	GND	NA	-	0V0	NA		GROUND	Ground
J4	78	XMIPI0SDPCLK	MIPI	-	1V0	NA		CAMERA	CSI0 PCLK
J4	80	XMIPI0SDNCLK	MIPI	-	1V0	NA		CAMERA	CSI0 NCLK

In *Figure 5* a listing of all power/signal names that are assigned to physical pins of connector J1 and connector J9 are given. In *Table 3* and *Table 4* the functions and electrical limitations associated with physical behavior of the pins is described. Functionally Connector J1 carries the following interfaces: USB3.0 DRD, USB HOST, MMC, I^2C and HDMI. Functionally Connector J9 carries JTAG functionality for the various devices. Again as with previous connectors the Interrupts, GPIO and I^2C functionality that is present on the connector's might be support for other interfaces present on the connector.

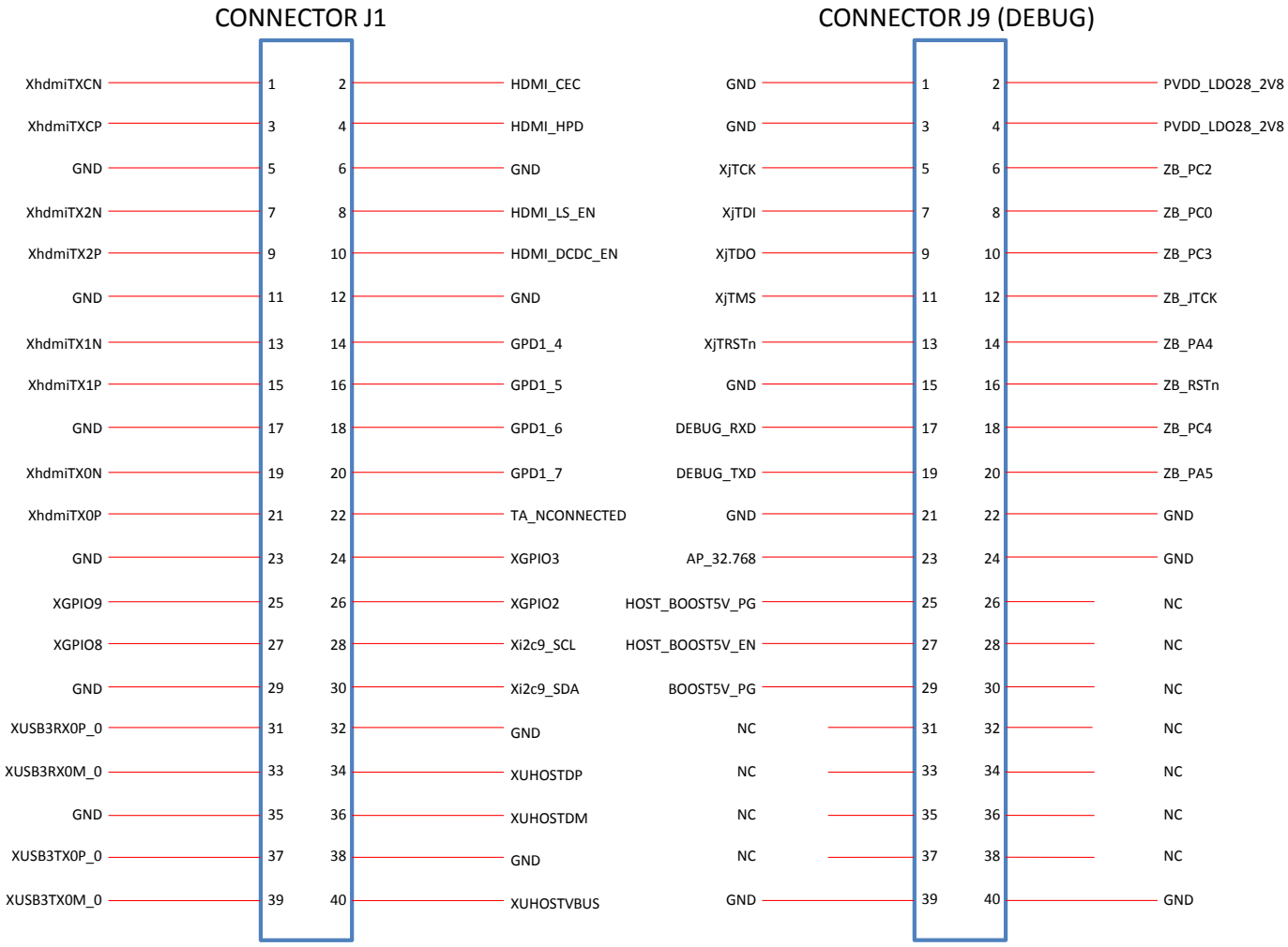


Figure 5. Connector J1, J9 Pin Layout

CONNECTOR J1

Table 3. Connector J1 Pin Description

Connector J1									
Conn#	Pin#	Name	I/O Type	Default	Voltage	DS [mA]	PUD*	Group	Function
J1	1	XhdmiTXCN	HDMI	-	1V0	NA		HDMI	TXCN
J1	3	XhdmiTXCP	HDMI	-	1V0	NA		HDMI	TXCP
J1	5	GND	NA	-	0V0	NA		GROUND	Ground
J1	7	XhdmiTX2N	HDMI	-	1V0	NA		HDMI	TX2N
J1	9	XhdmiTX2P	HDMI	-	1V0	NA		HDMI	TX2P
J1	11	GND	NA	-	0V0	NA		GROUND	Ground
J1	13	XhdmiTX1N	HDMI	-	1V0	NA		HDMI	TX1N
J1	15	XhdmiTX1P	HDMI	-	1V0	NA		HDMI	TX1P
J1	17	GND	NA	-	0V0	NA		GROUND	Ground
J1	19	XhdmiTX0N	HDMI	-	1V0	NA		HDMI	TXON
J1	21	XhdmiTX0P	HDMI	-	1V0	NA		HDMI	TXOP
J1	23	GND	NA	-	0V0	NA		GROUND	Ground
J1	25	XGPIO9	A	I	1V8	2	PDE	SIGFOX	Power enable
J1	27	XGPIO8	A	I	1V8	2	PDE	ZWAVE	Reset
J1	29	GND	NA	-	0V0	NA		GROUND	Ground
J1	31	XUSB3RX0P_0	USB3.0	-	1V0	NA		USB3.0	USB3.0 DRD channel 0 receive plus
J1	33	XUSB3RX0M_0	USB3.0	-	1V0	NA		USB3.0	USB3.0 DRD channel 0 receive minus
J1	35	GND	NA	-	0V0	NA		GROUND	Ground
J1	37	XUSB3TX0P_0	USB3.0	-	1V0	NA		USB3.0	USB3.0 DRD channel 0 transmit plus
J1	39	XUSB3TX0M_0	USB3.0	-	1V0	NA		USB3.0	USB3.0 DRD channel 0 transmit minus
J1	2	HDMI_CEC	A	I	1V8	2	PDE	HDMI	HDMI_CEC
J1	4	HDMI_HPD	A	EXT_INT43[7]	1V8	2	PDE	HDMI	HDMI_HPD
J1	6	GND	NA	-	0V0	NA		GROUND	Ground
J1	8	HDMI_LS_EN	A	O	1V8	2	PDE	HDMI	HDMI_LS_EN
J1	10	HDMI_DCDC_EN	A	O	1V8	2	PDE	HDMI	HDMI_DCDC_EN
J1	12	GND	NA		0V0	NA		GROUND	Ground
J1	14	GPD1_4	A	I	1V8	2	PDE	PROCESSOR	GENERIC DATA0
J1	16	GPD1_5	A	I	1V8	2	PDE	PROCESSOR	GENERIC DATA1
J1	18	GPD1_6	A	I	1V8	2	PDE	PROCESSOR	GENERIC DATA2
J1	20	GPD1_7	A	O	1V8	2	PDE	PROCESSOR	GENERIC DATA3
J1	22	TA_nCONNECTED	PMIC	-	1V8	NA		PMIC	Power up event
J1	24	XGPIO3	A	I	1V8	2	PDE	SIGFOX	GENERIC GPIO
J1	26	XGPIO2	A	I	1V8	2	PDE	CAMERA	GENERIC GPIO
J1	28	Xi2c9_SCL	A	I	1V8	2	PDE	Wi-Fi/BT	GENERIC SCL
J1	30	Xi2c9_SDA	A	I	1V8	2	PDE	Wi-Fi/BT	GENERIC SDA
J1	32	GND	NA	-	0V0	NA		GROUND	Ground
J1	34	XUHOSTDP	USB HOST	-	3V3	NA		USB/ETHERNET	USB data plus
J1	36	XUHOSTDM	USB HOST	-	3V3	NA		USB/ETHERNET	USB data minus
J1	38	GND	NA	-	0V0	NA		GROUND	Ground
J1	40	XUHOSTVBUS	USB HOST	-	3V3	NA		USB	USB vbus

CONNECTOR J9

Table 4. Connector J9 (Debug) Pin Description

Connector J9 (Debug)									
Conn#	Pin#	Name	I/O Type	Default	Voltage	DS [mA]	PUD*	Group	Function
J9	1	GND	NA	-	0V0	NA		GROUND	Ground
J9	3	GND	NA	-	0V0	NA		GROUND	Ground
J9	5	XjTCK	JTAG	-	1V8	NA		DEBUG	TCK
J9	7	XjTDI	JTAG	-	1V8	NA		DEBUG	TDI
J9	9	XjTDO	JTAG	-	1V8	NA		DEBUG	TDO
J9	11	XjTMS	JTAG	-	1V8	NA		DEBUG	TMS
J9	13	XjTRSTn	JTAG	-	1V8	NA		DEBUG	RSTn
J9	15	GND	NA	-	0V0	NA		GROUND	Ground
J9	17	DEBUG_RXD	A	UART_3_RXD	1V8	2	PUDD	USB	DEBUG RXD
J9	19	DEBUG_TXD	A	UART_3_TXD	1V8	2	PUDD	USB	DEBUG TXD
J9	21	GND	NA	-	0V0	NA		GROUND	Ground
J9	23	AP_32.768	PMIC	-	1V6*	NA		Wi-Fi/BT	32MHz clock signal
J9	25	HOST_BOOST5V_PG	A	I	1V8	2	PDE	NA	Host boost PG
J9	27	HOST_BOOST5V_EN	A	O	1V8	2	PDE	NA	Host boost Enable
J9	29	BOOST5V_PG	A	I	1V8	2	PDE	NA	Boost PG
J9	31	NC	NA	-	NA	-	-	-	Not connected
J9	33	NC	NA	-	NA	-	-	-	Not connected
J9	35	NC	NA	-	NA	-	-	-	Not connected
J9	37	NC	NA	-	NA	-	-	-	Not connected
J9	39	GND	NA	-	0V0	NA		GROUND	Ground
J9	2	PVDD_LDO28_2V8	PMIC	-	2V8	-	-	DEBUG	Zigbee power supply
J9	4	PVDD_LDO28_2V8	PMIC	-	2V8	-	-	DEBUG	Zigbee power supply
J9	6	ZB_PC2	ZIGBEE		1V8	4		DEBUG	JTAG data out
J9	8	ZB_PC0	ZIGBEE		1V8	8		DEBUG	JTAG reset
J9	10	ZB_PC3	ZIGBEE		1V8	4		DEBUG	JTAG data in
J9	12	ZB_JTCK	ZIGBEE		1V8	NA		DEBUG	JTAG TCK
J9	14	ZB_PA4	ZIGBEE		1V8	4		DEBUG	JTAG mode select
J9	16	ZB_RSTn	A/ZIGBEE	I	1V8	2	PDE	DEBUG	JTAG reset
J9	18	ZB_PC4	ZIGBEE		1V8	4		DEBUG	GPIO
J9	20	ZB_PA5	A/ZIGBEE	I	1V8	4		DEBUG	GPIO
J9	22	GND	NA	-	0V0	NA		GROUND	Ground
J9	24	GND	NA	-	0V0	NA		GROUND	Ground
J9	26	NC	NA	-	NA	-	-	-	Not connected
J9	28	NC	NA	-	NA	-	-	-	Not connected
J9	30	NC	NA	-	NA	-	-	-	Not connected
J9	32	NC	NA	-	NA	-	-	-	Not connected
J9	34	NC	NA	-	NA	-	-	-	Not connected
J9	36	NC	NA	-	NA	-	-	-	Not connected
J9	38	NC	NA	-	NA	-	-	-	Not connected
J9	40	GND	NA	-	0V0	NA		GROUND	Ground

ARTIK 102020 Module Functional Interfaces

This section describes the functional interfaces that can be found on the ARTIK 1020 Module. It is a subset of what is described in the previous section and as such not all pins will be described.

USB3.0 Functional Interface

Table 5. USB3.0 Functional Interface

USB3.0							
Conn#	Pin#	Name	I/O	I/O Type	Voltage	Group	Function
J3	20	DRD_VBUS_SENSE_0	I	A	1V8	USB3.0	DRD_VBUS_SENSE_0
J3	60	XUSB3VBUS0_0	I/O	USB3.0	3V3	USB3.0	USB3.0 DRD channel 0
J3	62	XUSB3ID0_0	I/O	A/USB3.0/ADC	1V8	USB3.0	Identification USB3.0 DRD channel 0
J3	66	XUSB3DP0_0	O	USB3.0	3V3	USB3.0	USB2.0 backward compatible P channel in USB3.0
J3	68	XUSB3DM0_0	O	USB3.0	3V3	USB3.0	USB2.0 backward compatible M channel in USB3.0
J4	55	BOOST5V_EN	O	A	1V8	USB3.0	USB3.0
J4	77	UDRD3_0_OVERCUR_U2	O	USB3.0	1V8	USB3.0	Control for USB3.0 DRD channel 0
J4	79	UDRD3_0_VBUSCTRL_U2	O	USB3.0	1V8	USB3.0	Control for USB3.0 DRD channel 0
J1	31	XUSB3RX0P_0	O	USB3.0	1V0	USB3.0	USB3.0 DRD channel 0 receive plus
J1	33	XUSB3RX0M_0	O	USB3.0	1V0	USB3.0	USB3.0 DRD channel 0 receive minus
J1	37	XUSB3TX0P_0	O	USB3.0	1V0	USB3.0	USB3.0 DRD channel 0 transmit plus
J1	39	XUSB3TX0M_0	O	USB3.0	1V0	USB3.0	USB3.0 DRD channel 0 transmit minus

Audio Functional Interface

Table 6. Audio Functional Interface

Audio							
Conn#	Pin#	Name	I/O	I/O Type	Voltage	Group	Function
J3	35	XEINT_27	I	A	1V8	AUDIO	JACK_DET
J3	67	XCLKOUT	O	NA	1V8	AUDIO	24MHz CDCLK
J3	75	Xi2c1_SCL	O	A	1V8	Wi-Fi/BT/AUDIO	SCL for BT audio
J3	77	Xi2c1_SDA	O	A	1V8	Wi-Fi/BT/AUDIO	SDA for BT audio
J3	72	xAudi2s0SDO	O	A	1V8	Wi-Fi/BT/AUDIO	Audio SDO
J3	74	xAudi2s0SDI	I	A	1V8	Wi-Fi/BT/AUDIO	Audio SDI
J3	76	xAudi2s0SCLK	O	A	1V8	Wi-Fi/BT/AUDIO	Audio SCLK
J3	78	xAudi2s0LRCK	O	A	1V8	Wi-Fi/BT/AUDIO	Audio LRCK
J3	80	xAudi2s0CDCLK	O	A	1V8	Wi-Fi/BT/AUDIO	Audio DCLK
J4	7	CODEC_PDN		A	1V8	Wi-Fi/BT/AUDIO	Codec Power Down

UARTS Functional Interface

Table 7. UARTS Functional Interface

UARTS							
Conn#	Pin#	Name	I/O	I/O Type	Voltage	Group	Function
J3	25	XEINT_18	I	A	1V8	UARTS	XUART_RST
J3	27	XEINT_20	I	A	1V8	UARTS	XUART_IRQ
J3	49	XUART_SCLK	I/O	A	1V8	UARTS	GENERIC UART SCLK

UARTS							
Conn#	Pin#	Name	I/O	I/O Type	Voltage	Group	Function
J3	51	XUART_MOSI	I/O	A	1V8	UARTS	GENERIC UART MOSI
J3	53	XUART_MISO	I/O	A	1V8	UARTS	GENERIC UART MISO
J3	55	XUART_CS	I/O	A	1V8	UARTS	GENERIC UART CS

Camera Functional Interface

Table 8. CAMERA Functional Interface

CAMERA							
Conn#	Pin#	Name	I/O	I/O Type	Voltage	Group	Function
J3	47	XGPIO1	O	A	1V8	CAMERA	Power down
J3	38	XCIS_MCLK	O	A	1V8	CAMERA	MCLK
J3	40	GPIO6/XT_INT156	O	A	1V8	CAMERA	MCLK
J4	1	MAINCAM_RESET	I	A	1V8	CAMERA	Reset
J4	3	CAM_FLASH_EN	O	A	1V8	CAMERA	Flash
J4	5	CAM_FLASH_TORCH	O	A	1V8	CAMERA	Flash torch
J4	17	VTCAM_RESET	I	A	1V8	CAMERA	Reset
J4	19	XISP2_SDA	I	A	1V8	CAMERA	SDA
J4	21	XISP2_SCL	I	A	1V8	CAMERA	SCL
J4	25	XMIPI1SDN0	I	MIPI	1V0	CAMERA	CSI1 SDN0 CHANNEL 0
J4	27	XMIPI1SDP0	I	MIPI	1V0	CAMERA	CSI1 SDP0 CHANNEL 0
J4	31	XMIPI1SDN1	I	MIPI	1V0	CAMERA	CSI1 SDN1 CHANNEL 1
J4	33	XMIPI1SDP1	I	MIPI	1V0	CAMERA	CSI1 SDP1 CHANNEL 1
J4	37	XMIPI1SDNCLK	O	MIPI	1V0	CAMERA	CSI1 SDNCLK
J4	39	XMIPI1SDPCLK	O	MIPI	1V0	CAMERA	CSI1 SDPCLK
J4	49	XISP0_SCL	I	A	1V8	CAMERA	SCL
J4	51	XISP0_SDA	I	A	1V8	CAMERA	SDA
J4	54	XMIPI0SDN0	I	MIPI	1V0	CAMERA	CSI0 DN0 CHANNEL 0
J4	56	XMIPI0SDP0	I	MIPI	1V0	CAMERA	CSI0 DP0 CHANNEL 0
J4	60	XMIPI0SDN1	I	MIPI	1V0	CAMERA	CSI0 DN1 CHANNEL 1
J4	62	XMIPI0SDP1	I	MIPI	1V0	CAMERA	CSI0 DP1 CHANNEL 1
J4	66	XMIPI0SDN2	I	MIPI	1V0	CAMERA	CSI0 DN2 CHANNEL 2
J4	68	XMIPI0SDP2	I	MIPI	1V0	CAMERA	CSI0 DP2 CHANNEL 2
J4	72	XMIPI0SDN3	I	MIPI	1V0	CAMERA	CSI0 DN3 CHANNEL 3
J4	74	XMIPI0SDP3	I	MIPI	1V0	CAMERA	CSI0 DP3 CHANNEL 3
J4	78	XMIPI0SDPCLK	O	MIPI	1V0	CAMERA	CSI0 PCLK
J4	80	XMIPI0SDNCLK	O	MIPI	1V0	CAMERA	CSI0 NCLK
J1	26	XGPIO2	I/O	A	1V8	CAMERA	GENERIC GPIO

SD Card Functional Interface

Table 9. SD Card Functional Interface

SD CARD							
Conn#	Pin#	Name	I/O	I/O Type	Voltage	Group	Function
J4	32	XMMC2CDN	I	B	2V8	SD CARD	CDN card detect
J4	34	XMMC2CLK	O	B	2V8	SD CARD	CLK
J4	36	XMMC2CMD	I/O	B	2V8	SD CARD	CMD
J4	38	XMMC2DATA0	I/O	B	2V8	SD CARD	DATA0
J4	40	XMMC2DATA1	I/O	B	2V8	SD CARD	DATA1

SD CARD							
Conn#	Pin#	Name	I/O	I/O Type	Voltage	Group	Function
J4	42	XMMC2DATA2	I/O	B	2V8	SD CARD	DATA2
J4	44	XMMC2DATA3	I/O	B	2V8	SD CARD	DATA3

Power/Reset Functional Interface

Table 10. Power/Reset Functional Interface

Power/Reset							
Conn#	Pin#	Name	I/O	I/O Type	Voltage	Group	Function
J3	23	XEINT_17	I	A	1V8	POWER/RESET	CHG_IRQ
J3	39	V_ADP_SENSE	?	A	1V8	POWER/RESET	V_ADP_SENSE
J3	43	XOM2	I	PROCESSOR	1V8	POWER/RESET	SDMMC_CH2 or eMMC44_CH0 boot
J3	45	XOM3	I	PROCESSOR	1V8	POWER/RESET	SDMMC_CH2 or eMMC44_CH0 boot
J3	71	Xi2c0_SCL	O	A	1V8	POWER/RESET	SCL
J3	73	Xi2c0_SDA	O	A	1V8	POWER/RESET	SDC
J3	16	PWR_KEY	I	PMIC	1V8	POWER/RESET	Power on, high active
J4	43	MRNRESET	O	PROCESSOR /PMIC	1V8	POWER/RESET/ARDUINO/ SENSOR/Wi-Fi/BT	PMIC resets Processor Subsystem
J4	63	CHG_SDA_1.8V	I	A	1V8	POWER/RESET	Change I2C to 1V8 signaling
J4	65	CHG_SCL_1.8V	I	A	1V8	POWER/RESET	Change I2C to 1V8 signaling
J4	46	GPIOC40	I	B	2V8	POWER/RESET	GPIO

LCD Functional Interface

Table 11. LCD Functional Interface

LCD							
Conn#	Pin#	Name	I/O	I/O Type	Voltage	Group	Function
J3	15	XEINT_12	I/O	A	1V8	LCD	MIPI error detection
J3	29	XEINT_21	I	A	1V8	LCD	TP_RST
J3	31	XEINT_24	I	A	1V8	LCD	TP_INT
J4	57	LCD_RST	I	A	1V8	LCD	Reset
J4	59	Xi2c8_SDA	O	A	1V8	LCD	SCL
J4	61	Xi2c8_SCL	O	A	1V8	LCD	SDA
J4	2	XMIPI1MDN0	O	MIPI	1V0	LCD	DSI1 DN0 CHANNEL 0
J4	4	XMIPI1MDP0	O	MIPI	1V0	LCD	DSI1 DP0 CHANNEL 0
J4	8	XMIPI1MDN1	O	MIPI	1V0	LCD	DSI1 DN1 CHANNEL 1
J4	10	XMIPI1MDP1	O	MIPI	1V0	LCD	DSI1 DP1 CHANNEL 1
J4	14	XMIPI1MDP2	O	MIPI	1V0	LCD	DSI1 DP2 CHANNEL 2
J4	16	XMIPI1MDN2	O	MIPI	1V0	LCD	DSI1 DN2 CHANNEL 2
J4	20	XMIPI1MDN3	O	MIPI	1V0	LCD	DSI1 DN3 CHANNEL 3
J4	22	XMIPI1MDP3	O	MIPI	1V0	LCD	DSI1 DP3 CHANNEL 3
J4	26	XMIPI1MDNCLK	O	MIPI	1V0	LCD	DSI1 NCLK
J4	28	XMIPI1MDPCLK	O	MIPI	1V0	LCD	DSI1 PCLK

USB/Ethernet Functional Interface

Table 12. USB/Ethernet Functional Interface

USB/Ethernet							
Conn#	Pin#	Name	I/O	I/O Type	Voltage	Group	Function
J4	75	XUHOSTPWREN	O	USB HOST	1V8	USB/ETHERNET	USB
J1	34	XUHOSTDP	I/O	USB HOST	3V3	USB/ETHERNET	USB data plus
J1	36	XUHOSTDM	I/O	USB HOST	3V3	USB/ETHERNET	USB data minus
J1	40	XUHOSTVBUS	O	USB HOST	3V3	USB	USB vbus
J9	17	DEBUG_RXD	I	A	1V8	USB	DEBUG RXD
J9	19	DEBUG_TXD	O	A	1V8	USB	DEBUG TXD

Arduino Functional Interface

Table 13. Arduino Functional Interface

Arduino							
Conn#	Pin#	Name	I/O	I/O Type	Voltage	Group	Function
J3	17	XEINT_13	I/O	A	1V8	ARDUINO	GPIO
J3	19	XEINT_14	I/O	A	1V8	ARDUINO	GPIO
J3	18	XEINT_8	I/O	A	1V8	ARDUINO	GPIO
J3	22	XEINT_6	I/O	A	1V8	ARDUINO	GPIO
J3	24	XEINT_5	I/O	A	1V8	ARDUINO	GPIO
J3	26	XEINT_4	I/O	A	1V8	ARDUINO	GPIO
J3	28	XEINT_3	I/O	A	1V8	ARDUINO	GPIO
J3	30	XEINT_2	I/O	A	1V8	ARDUINO	GPIO
J3	32	XEINT_1	I/O	A	1V8	ARDUINO	GPIO
J3	34	XEINT_0	I/O	A	1V8	ARDUINO	GPIO
J3	42	Xu1_RXD	I	A	1V8	ARDUINO	UART RXD
J3	44	Xu1_TXD	O	A	1V8	ARDUINO	UART TXD
J3	48	Xadc0AIN0	I	Analog	1V8	ARDUINO	ADC
J3	50	Xadc0AIN1	I	Analog	1V8	ARDUINO	ADC
J3	52	Xadc0AIN2	I	Analog	1V8	ARDUINO	ADC
J3	54	Xadc0AIN5	I	Analog	1V8	ARDUINO	ADC
J3	56	Xadc0AIN6	I	Analog	1V8	ARDUINO	ADC
J3	58	Xadc0AIN7	I	Analog	1V8	ARDUINO	ADC
J4	67	Xpwmo_1	O	A	1V8	ARDUINO	PWM On/Off control
J4	69	Xpwmo_0	O	A	1V8	ARDUINO	PWM On/Off control

HDMI Functional Interface

Table 14. HDMI Functional Interface

HDMI							
Conn#	Pin#	Name	I/O	I/O Type	Voltage	Group	Function
J4	48	Xi2c7_SDA	O	A	1V8	HDMI	SCL
J4	50	Xi2c7_SCL	O	A	1V8	HDMI	SDA
J1	1	XhdmiTXCN	O	HDMI	1V0	HDMI	TXCN

J1	3	XhdmiTXCP	O	HDMI	1V0	HDMI	TXCP
J1	7	XhdmiTX2N	O	HDMI	1V0	HDMI	TX2N
J1	9	XhdmiTX2P	O	HDMI	1V0	HDMI	TX2P
J1	13	XhdmiTX1N	O	HDMI	1V0	HDMI	TX1N
J1	15	XhdmiTX1P	O	HDMI	1V0	HDMI	TX1P
J1	19	XhdmiTX0N	O	HDMI	1V0	HDMI	TXON
J1	21	XhdmiTX0P	O	HDMI	1V0	HDMI	TXOP
J1	2	HDMI_CEC	O	A	1V8	HDMI	HDMI_CEC
J1	4	HDMI_HPD	O	A	1V8	HDMI	HDMI_HPD
J1	8	HDMI_LS_EN	O	A	1V8	HDMI	HDMI_LS_EN
J1	10	HDMI_DCDC_EN	O	A	1V8	HDMI	HDMI_DCDC_EN

SigFox Functional Interface

Table 15. SigFox Functional Interface

SigFox							
Conn #	Pin#	Name	I/O	I/O Type	Voltage	Group	Function
J3	59	XspiCLK1	I/O	A	1V8	Wi-Fi/BT/SIGFOX	SPI CLK
J3	61	XspiCSn1	I/O	A	1V8	SIGFOX	SPI CSn
J3	63	XspiMISO1	I/O	A	1V8	Wi-Fi/BT/SIGFOX	SPI MISO
J3	65	XspiMOSI1	I/O	A	1V8	Wi-Fi/BT/SIGFOX	SPI MOSI
J4	9	XGPIO17/XT_INT163	O	A	1V8	SIGFOX	Low power control
J4	45	LCD_ID	O	A	1V8	SIGFOX	Vsync
J1	25	XGPIO9	O	A	1V8	SIGFOX	Power enable
J1	24	XGPIO3	I/O	A	1V8	SIGFOX	GENERIC GPIO

Debug Functional Interface

Table 16. Debug Functional Interface

Debug							
Conn #	Pin#	Name	I/O	I/O Type	Voltage	Group	Function
J9	5	XjTCK	I	JTAG	1V8	DEBUG	TCK
J9	7	XjTDI	I	JTAG	1V8	DEBUG	TDI
J9	9	XjTDO	O	JTAG	1V8	DEBUG	TDO
J9	11	XjTMS	I	JTAG	1V8	DEBUG	TMS
J9	13	XjTRSTn	I	JTAG	1V8	DEBUG	RSTn
J9	2	PVDD_LDO28_2V8		PMIC	2V8	DEBUG	Zigbee power supply
J9	4	PVDD_LDO28_2V8		PMIC	2V8	DEBUG	Zigbee power supply
J9	6	ZB_PC2	O	ZIGBEE	1V8	DEBUG	JTAG data out
J9	8	ZB_PC0	I	ZIGBEE	1V8	DEBUG	JTAG reset
J9	10	ZB_PC3	I	ZIGBEE	1V8	DEBUG	JTAG data in
J9	12	ZB_JTCK	I	ZIGBEE	1V8	DEBUG	JTAG TCK
J9	14	ZB_PA4	I	ZIGBEE	1V8	DEBUG	JTAG mode select
J9	16	ZB_RSTn	I	A/ZIGBEE	1V8	DEBUG	JTAG reset
J9	18	ZB_PC4		ZIGBEE	1V8	DEBUG	GPIO
J9	20	ZB_PA5	I/O	A/ZIGBEE	1V8	DEBUG	GPIO

ARTIK 1020 GPIO Alternate Functions

The Type A and Type B GPIOs as indicated in the connector tables have alternate functions that can be programmed using the GPIO API provided in the SW development environment. The tables below provide the alternate functions of all Type A and Type B GPIO's that are available on the edge connectors that are not connected to other components on the ARTIK 1020 Module.

Table 17. Type A GPIO Alternate Functions Connector J3

Connector J3 Type A GPIO											
Conn#	Pin#	Name	DV	F0	F1	F2	F3	F4	F5	F6	F7
J3	15	XEINT_12	I	I	O	WAKEUP_INT1[4]	Reserved	TraceData[12]	ALV_DBG[8]	Reserved	EXT_INT41[4]
J3	17	XEINT_13	I	I	O	WAKEUP_INT1[5]	Reserved	TraceData[13]	ALV_DBG[9]	Reserved	EXT_INT41[5]
J3	19	XEINT_14	I	I	O	WAKEUP_INT1[6]	Reserved	TraceData[14]	ALV_DBG[10]	Reserved	EXT_INT41[6]
J3	21	XEINT_16	I	I	O	WAKEUP_INT2[0]	Reserved	TraceData[16]	ALV_DBG[12]	Reserved	EXT_INT42[0]
J3	23	XEINT_17	I	I	O	WAKEUP_INT2[1]	Reserved	TraceData[17]	ALV_DBG[13]	Reserved	EXT_INT42[1]
J3	25	XEINT_18	I	I	O	WAKEUP_INT2[2]	Reserved	TraceData[18]	ALV_DBG[14]	Reserved	EXT_INT42[2]
J3	27	XEINT_20	I	I	O	WAKEUP_INT2[4]	Reserved	TraceData[20]	ALV_DBG[16]	Reserved	EXT_INT42[4]
J3	29	XEINT_21	I	I	O	WAKEUP_INT2[5]	Reserved	TraceData[21]	ALV_DBG[17]	Reserved	EXT_INT42[5]
J3	31	XEINT_24	I	I	O	WAKEUP_INT3[0]	Reserved	TraceData[24]	ALV_DBG[20]	Reserved	EXT_INT43[0]
J3	33	UHOST_ID	EXT_INT43[1]	I	O	WAKEUP_INT3[1]	Reserved	TraceData[25]	ALV_DBG[21]	Reserved	EXT_INT43[1]
J3	35	XEINT_27	I	I	O	WAKEUP_INT3[3]	Reserved	TraceData[27]	ALV_DBG[23]	Reserved	EXT_INT43[3]
J3	37	XEINT_28	I	I	O	WAKEUP_INT3[4]	Reserved	TraceData[28]	ALV_DBG[24]	Reserved	EXT_INT43[4]
J3	39	V_ADP_SENSE	I	I	O	WAKEUP_INT1[2]	Reserved	TraceData[10]	ALV_DBG[6]	Reserved	EXT_INT41[2]
J3	47	XGPIO1	I	I	O	Reserved	Reserved	Reserved	Reserved	Reserved	EXT_INT15[1]
J3	49	XUART_SCLK	I	I	O	I2S_1_CDCLK	PCM_1_EXTCLK	Reserved	Reserved	Reserved	EXT_INT4[1]
J3	51	XUART_MOSI	I	I	O	I2S_1_SCLK	PCM_1_SCLK	Reserved	Reserved	Reserved	EXT_INT4[0]
J3	53	XUART_MISO	I	I	O	I2S_1_SDI	PCM_1_SIN	Reserved	Reserved	Reserved	EXT_INT4[3]
J3	55	XUART_CS	I	I	O	I2S_1_LRCK	PCM_1_FSYNC	Reserved	Reserved	Reserved	EXT_INT4[2]
J3	59	XspiCLK1	I	I	O	SPI_1_CLK	Reserved	Reserved	Reserved	Reserved	EXT_INT3[4]
J3	61	XspiCSn1	I	I	O	SPI_1_nSS	Reserved	Reserved	Reserved	Reserved	EXT_INT3[5]
J3	63	XspiMISO1	I	I	O	SPI_1_MISO	Reserved	Reserved	Reserved	Reserved	EXT_INT3[6]
J3	65	XspiMOSI1	I	I	O	SPI_1_MOSI	Reserved	Reserved	Reserved	Reserved	EXT_INT3[7]
J3	71	Xi2c0_SCL	I	I	O	I2C_0_SCL	Reserved	Reserved	Reserved	Reserved	EXT_INT7[1]
J3	73	Xi2c0_SDA	I	I	O	I2C_0_SDA	Reserved	Reserved	Reserved	Reserved	EXT_INT7[0]
J3	75	Xi2c1_SCL	I2C_1_SCL	I	O	I2C_1_SCL	MIPI1_ESC_CLK	Reserved	Reserved	Reserved	EXT_INT7[3]
J3	77	Xi2c1_SDA	I2C_1_SDA	I	O	I2C_1_SDA	MIPI1_BYTE_CLK	Reserved	Reserved	Reserved	EXT_INT7[2]
J3	18	XEINT_8	I	I	O	WAKEUP_INT1[0]	Reserved	TraceData[8]	ALV_DBG[4]	Reserved	EXT_INT41[0]
J3	20	DRD_VBUS_SENSE_0	EXT_INT40[7]	I	O	WAKEUP_INT0[7]	DP0_HPD	Reserved	ALV_DBG[3]	Reserved	EXT_INT40[7]
J3	22	XEINT_6	I	I	O	WAKEUP_INT0[6]	Reserved	Reserved	ALV_DBG[2]	Reserved	EXT_INT40[6]
J3	24	XEINT_5	I	I	O	WAKEUP_INT0[5]	Reserved	Reserved	ALV_DBG[1]	MFC_RTCK	EXT_INT40[5]
J3	26	XEINT_4	I	I	O	WAKEUP_INT0[4]	Reserved	Reserved	ALV_DBG[0]	MFC_TRSTn	EXT_INT40[4]
J3	28	XEINT_3	I	I	O	WAKEUP_INT0[3]	Reserved	Reserved	ALV_TDO	MFC_TDO	EXT_INT40[3]
J3	30	XEINT_2	I	I	O	WAKEUP_INT0[2]	Reserved	Reserved	ALV_TDI	MFC_TDI	EXT_INT40[2]
J3	32	XEINT_1	I	I	O	WAKEUP_INT0[1]	Reserved	Reserved	ALV_TMS	MFC_TMS	EXT_INT40[1]

Connector J3 Type A GPIO											
Conn#	Pin#	Name	DV	F0	F1	F2	F3	F4	F5	F6	F7
J3	34	XEINT_0	I	I	O	WAKEUP_INT0[0]	Reserved	Reserved	ALV_TCK	MFC_TCK	EXT_INT40[0]
J3	38	XCIS_MCLK	I	I	O	CIS_CLK0	Reserved	Reserved	Reserved	Reserved	EXT_INT15[5]
J3	40	GPIO6/ XT_INT156	I	I	O	CIS_CLK1	Reserved	Reserved	Reserved	Reserved	EXT_INT15[6]
J3	42	Xu1_RXD	UART_ 1_RXD	I	O	UART_1_RXD	Reserved	Reserved	Reserved	Reserved	EXT_INT1[4]
J3	44	Xu1_TXD	UART_ 1_TXD	I	O	UART_1_TXD	Reserved	Reserved	Reserved	Reserved	EXT_INT1[5]
J3	72	xAudi2s0SD O		I	O	AUD_I2S_0_SDO[0]	AUD_PCM _0_ SOUT	Reserved	Reserved	Reserved	EXT_INT50[4]
J3	74	xAudi2s0SDI		I	O	AUD_I2S_0_SDI	AUD_PCM _0_ SIN	Reserved	Reserved	Reserved	EXT_INT50[3]
J3	76	xAudi2s0SCL K		I	O	AUD_I2S_0_SCLK	AUD_PCM _0_ SCLK	Reserved	Reserved	Reserved	EXT_INT50[0]
J3	78	xAudi2s0LRC K		I	O	AUD_I2S_0_LRCK	AUD_PCM _0_ FSYNC	Reserved	Reserved	Reserved	EXT_INT50[2]
J3	80	xAudi2s0CDC LK		I	O	AUD_I2S_0_CDCL K	AUD_PCM _0_ EXTCLK	Reserved	Reserved	Reserved	EXT_INT50[1]

Table 18. Type A GPIO Alternate Functions Connector J4

Connector J4 Type A GPIO											
Conn#	Pin#	Name	DV	F0	F1	F2	F3	F4	F5	F6	F7
J4	1	MAINCAM_ RESET	I	I	O	CAM_GPIO[1]	MPWM2_OUT_IS P	Reserved	TEST_DPTX_ PLLOUTDIV08	Reserved	EXT_INT17[1]
J4	3	CAM_FLASH_ EN	O	I	O	CAM_GPIO[2]	MPWM3_OUT_IS P	Reserved	DP1_CH0_TXD_ CLK_DIV08	Reserved	EXT_INT17[2]
J4	5	CAM_FLASH_ TORCH	O	I	O	CAM_GPIO[3]	MPWM4_OUT_IS P	Reserved	DP1_CH1_TXD_ CLK_DIV08	Reserved	EXT_INT17[3]
J4	7	CODEC_PDN	O	I	O	Reserved	Reserved	Reserved	Reserved	Reserved	EXT_INT16[2]
J4	9	XGPIO17/ XT_INT163	I	I	O	Reserved	Reserved	Reserved	Reserved	Reserved	EXT_INT16[3]
J4	11	PSR_TE	I	I	O	FIMD1_DDI_SYN C	Reserved	Reserved	Reserved	Reserved	EXT_INT16[0]
J4	13	SEQ_I2C_SCL	I	I	O	SPI_0_MOSI	HS_I2C_5_SCL	Reserved	Reserved	Reserved	EXT_INT3[3]
J4	15	SEQ_I2C_SDA	I	I	O	SPI_0_MISO	HS_I2C_5_SDA	Reserved	Reserved	Reserved	EXT_INT3[2]
J4	17	VTCAM_RESE T	I	I	O	CAM_GPIO[4]	MPWM5_OUT_IS P	CAM_SPI1_MIS O	DP1_CH2_TXD_ CLK_DIV08	Reserved	EXT_INT17[4]
J4	19	XISP2_SDA	I	I	O	CAM_I2C2_SDA	Reserved	Reserved	Reserved	Reserved	EXT_INT19[4]
J4	21	XISP2_SCL	I	I	O	CAM_I2C2_SCL	Reserved	Reserved	Reserved	Reserved	EXT_INT19[5]
J4	45	LCD_ID	I	I	O	SROM_DATA[2]	Reserved	Reserved	Reserved	Reserved	Reserved
J4	49	XISP0_SCL	I	I	O	CAM_I2C0_SCL	CAM_GPIO[11]	Reserved	Reserved	Reserved	EXT_INT19[1]
J4	51	XISP0_SDA	I	I	O	CAM_I2C0_SDA	CAM_GPIO[10]	Reserved	Reserved	Reserved	EXT_INT19[0]
J4	55	BOOST5V_EN	O	I	O	SROM_DATA[10]	Reserved	Reserved	Reserved	Reserved	Reserved
J4	57	LCD_RST	I	I	O	SROM_nWBE[0]	Reserved	Reserved	Reserved	Reserved	Reserved
J4	59	Xi2c8_SDA	I	I	O	HS_I2C_8_SDA	Reserved	Reserved	Reserved	Reserved	EXT_INT7[4]

Connector J4 Type A GPIO											
Conn#	Pin#	Name	DV	F0	F1	F2	F3	F4	F5	F6	F7
J4	61	Xi2c8_SCL	I	I	O	HS_I2C_8_SCL	Reserved	Reserved	Reserved	Reserved	EXT_INT7[5]
J4	63	CHG_SDA_1.8V	I	I	O	SROM_GnCS[2]	Reserved	Reserved	Reserved	Reserved	Reserved
J4	65	CHG_SCL_1.8V	I	I	O	SROM_GnCS[3]	Reserved	Reserved	Reserved	Reserved	Reserved
J4	67	Xpwmo_1	I	I	O	TOUT_1	Reserved	Reserved	Reserved	Reserved	EXT_INT6[1]
J4	69	Xpwmo_0	I	I	O	TOUT_0	LCD_B_PWM	Reserved	Reserved	Reserved	EXT_INT6[0]
J4	48	Xi2c7_SDA	I	I	O	TOUT_2	HS_I2C_7_SDA	Reserved	Reserved	Reserved	EXT_INT6[2]
J4	50	Xi2c7_SCL	I	I	O	TOUT_3	HS_I2C_7_SCL	Reserved	Reserved	Reserved	EXT_INT6[3]

Table 19. Type A GPIO Alternate Functions Connector J1

Connector J1 Type A GPIO											
Conn#	Pin#	Name	DV	F0	F1	F2	F3	F4	F5	F6	F7
J1	25	XGPIO9	I	I	O	Reserved	Reserved	TraceData[1]	Reserved	Reserved	EXT_INT24[1]
J1	27	XGPIO8	I	I	O	Reserved	Reserved	TraceData[0]	Reserved	Reserved	EXT_INT24[0]
J1	2	HDMI_CEC	I	I	O	WAKEUP_INT3[6]	HDMI_CEC	TraceData[30]	ALV_DBG[26]	Reserved	EXT_INT43[6]
J1	4	HDMI_HPD	EXT_INT43[7]	I	O	WAKEUP_INT3[7]	HDMI_HPD	TraceData[31]	ALV_DBG[27]	Reserved	EXT_INT43[7]
J1	8	HDMI_LS_EN	O	I	O	SROM_ADDR[10]	Reserved	Reserved	Reserved	Reserved	Reserved
J1	10	HDMI_DCDC_EN	O	I	O	SROM_ADDR[11]	Reserved	Reserved	Reserved	Reserved	Reserved
J1	14	GPD1_4	I	I	O	SD_1_DATA[4]	Reserved	Reserved	Reserved	Reserved	EXT_INT14[4]
J1	16	GPD1_5	I	I	O	SD_1_DATA[5]	Reserved	Reserved	Reserved	Reserved	EXT_INT14[5]
J1	18	GPD1_6	I	I	O	SD_1_DATA[6]	Reserved	Reserved	Reserved	Reserved	EXT_INT14[6]
J1	20	GPD1_7	O	I	O	SD_1_DATA[7]	Reserved	Reserved	Reserved	Reserved	EXT_INT14[7]
J1	24	XGPIO3	I	I	O	Reserved	Reserved	Reserved	Reserved	Reserved	EXT_INT15[3]
J1	26	XGPIO2	I	I	O	Reserved	Reserved	Reserved	Reserved	Reserved	EXT_INT15[2]
J1	28	Xi2c9_SCL	I	I	O	HS_I2C_9_SCL	DISP1_HSYNC	Reserved	Reserved	Reserved	EXT_INT7[7]
J1	30	Xi2c9_SDA	I	I	O	HS_I2C_9_SDA	Reserved	Reserved	Reserved	Reserved	EXT_INT7[6]

Table 20. Type A GPIO Alternate Functions Connector J9

Connector J9 Type A GPIO											
Conn#	Pin#	N ame	DV	F0	F1	F2	F3	F4	F5	F6	F7
J9	17	DEBUG_RXD	UART_3_RXD	I	O	UART_3_RXD	Reserved	UART_AUDIO_RXD	Reserved	Reserved	EXT_INT2[4]
J9	19	DEBUG_TXD	UART_3_TXD	I	O	UART_3_TXD	Reserved	UART_AUDIO_TXD	Reserved	Reserved	EXT_INT2[5]
J9	25	HOST_BOOST5V_PG	I	I	O	SROM_DATA[13]	Reserved	Reserved	Reserved	Reserved	Reserved
J9	27	HOST_BOOST5V_EN	O	I	O	SROM_DATA[12]	Reserved	Reserved	Reserved	Reserved	Reserved
J9	29	BOOST5V_PG	I	I	O	SROM_DATA[11]	Reserved	Reserved	Reserved	Reserved	Reserved

Table 21. Type B GPIO Alternate Functions Connector J4

Connector J4 Type B GPIO											
Conn#	Pin#	Name	DV	F0	F1	F2	F3	F4	F5	F6	F7
J4	32	XMMC2CDN		I	O	SD_2_CDn	Reserved	Reserved	Reserved	Reserved	EXT_INT11[2]
J4	34	XMMC2CLK		I	O	SD_2_CLK	Reserved	Reserved	Reserved	Reserved	EXT_INT11[0]

Connector J4 Type B GPIO											
Conn#	Pin#	Name	DV	F0	F1	F2	F3	F4	F5	F6	F7
J4	36	XMMC2CMD		I	O	SD_2_CMD	Reserved	Reserved	Reserved	Reserved	EXT_INT11[1]
J4	38	XMMC2DATA0		I	O	SD_2_DATA[0]	Reserved	Reserved	Reserved	Reserved	EXT_INT11[3]
J4	40	XMMC2DATA1		I	O	SD_2_DATA[1]	Reserved	Reserved	Reserved	Reserved	EXT_INT11[4]
J4	42	XMMC2DATA2		I	O	SD_2_DATA[2]	Reserved	Reserved	Reserved	Reserved	EXT_INT11[5]
J4	44	XMMC2DATA3		I	O	SD_2_DATA[3]	Reserved	Reserved	Reserved	Reserved	EXT_INT11[6]
J4	46	GPIOC40	I	I	O	SD_2_WP	Reserved	Reserved	Reserved	Reserved	EXT_INT13[0]

ARTIK 1020 Module Booting Sequence

During system reset, the program that is stored in iROM (internal ROM), that is part of the ARTIK 1020 Module, is executes from address 0x0000_0000. The iROM area is by default mapped to this address. The system reset may be asserted during the time of booting and wakeup by using low power modes, as a consequence the boot loader executes appropriate processes according to the reset status. There are 2 boot loaders to initiate a first and a second boot, implemented according to a typical bootstrap loading procedure.

Typically there are 4 steps in the ARTIK 1020 Module booting process:

1. After reset the iROM code, that contains a small program to initialize the processor subsystem, is executed.
   The iROM is an internal 64 KB ROM, it initializes basic system functions such as Clock and Stack and it initializes the SD/MMC controller. The iROM code is also responsible for also loading the Boot Loader 1 (BL1) image from either the 16GB MLCX2 flash or from an external memory device, to the internal SRAM (iSRAM). The iROM code verifies the BL1 image to assure that the image is authentic and that the calculated hash is associated with the preset secure boot key. As a last step the iROM code jumps to the start of the BL1 code so that execution of the BL1 code can start.
2. The BL1 is still an ARTIK 1020 Module specific boot. The BL1 code that was transferred to the local iSRAM using the iROM executable is now executed and it will start initializing the system clocks and the DRAM controller. Now the BL2 code can be loaded into DRAM and executed from there. As a last step the BL1 code will jump to the start of the BL2 code so that execution of the BL2 code can start from DRAM.
3. The BL2 will now load the OS into DRAM and control will be transferred to the OS.
4. The OS has started upon completion of the boot process and can load a specific IoT application that will, as part of its function, initialize Bluetooth, ZigBee etc, before it executes its specific IoT task.

The type of booting can be determined by changing the levels of 2 pins on Connector J3:[43,45]. *Table 22*, provides the 2 booting options that are available. If the first device choice does not work to boot up the ARTIK 1020 Module, the second device choice will be tried automatically.

Table 22. Booting Options

J3:[45,43]	First Device	Second Device
2b'01	SDMMC_CH2	USB
2b'10	eMMC44_CH0	USB

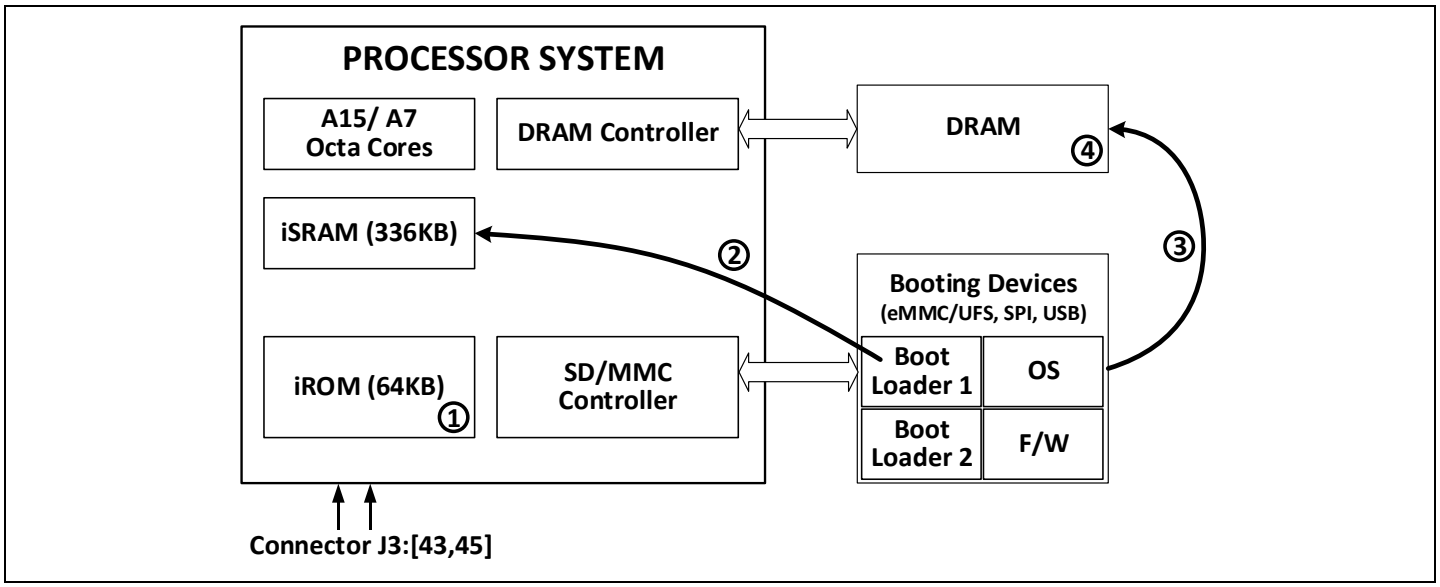


Figure 6. ARTIK 1020 Module Booting Sequence

ARTIK 1020 Module Reset Scenarios

There are 5 different reset scenarios that are supported on the ARTIK 1020 Module namely:

- Hardware reset
- Watchdog reset
- Software reset
- Wake up from SLEEP
- Wake up from DEEP-STOP

Table 23, lists the mandatory functions that will be executed per reset scenario.

Table 23. Required Functions per Reset Type

Reset Type	Initialization in iROM	PLL Setting in iROM	BL1 Execution	PLL and DRAM Setting in BL1	OS Loading	Restore Previous State
Hardware Reset	–	–	–	–	–	X
Watchdog Reset	–	–	–	–	–	X
Software Reset	–	–	–	–	–	X
Wake up from SLEEP	–	–	–	–	X	–
Wake up from DEEP-STOP	–	X(1)	X	–	X	–
Wake up from Low Power Audio (LPA)	–	X(1)	X	–	X	–

1. During software reset, the contents of the internal SRAM and the external DRAM are preserved. However, when waking up from a DEEP-STOP, BL1, BL2 and the OS must be loaded to ensure software integrity. SRAM is preserved in this mode and as such it is not required to reload the boot loader.
2. X means action will take place after particular Reset Type.

ARTIK 1020 Module Antenna Connections

Two antennas are required to use the full set of radio communication links on the ARTIK 1020 Module. One supports the combination of Wi-Fi and BT, and the other is dedicated to ZigBee.

Caution: Do not apply power (enable) the radio chips before connecting antennas or damage to the chip may result.

The U.FL-R-SMT Hirose connector is used for both the BT/Wi-Fi and the ZigBee antenna connectors on the ARTIK 1020 Module.

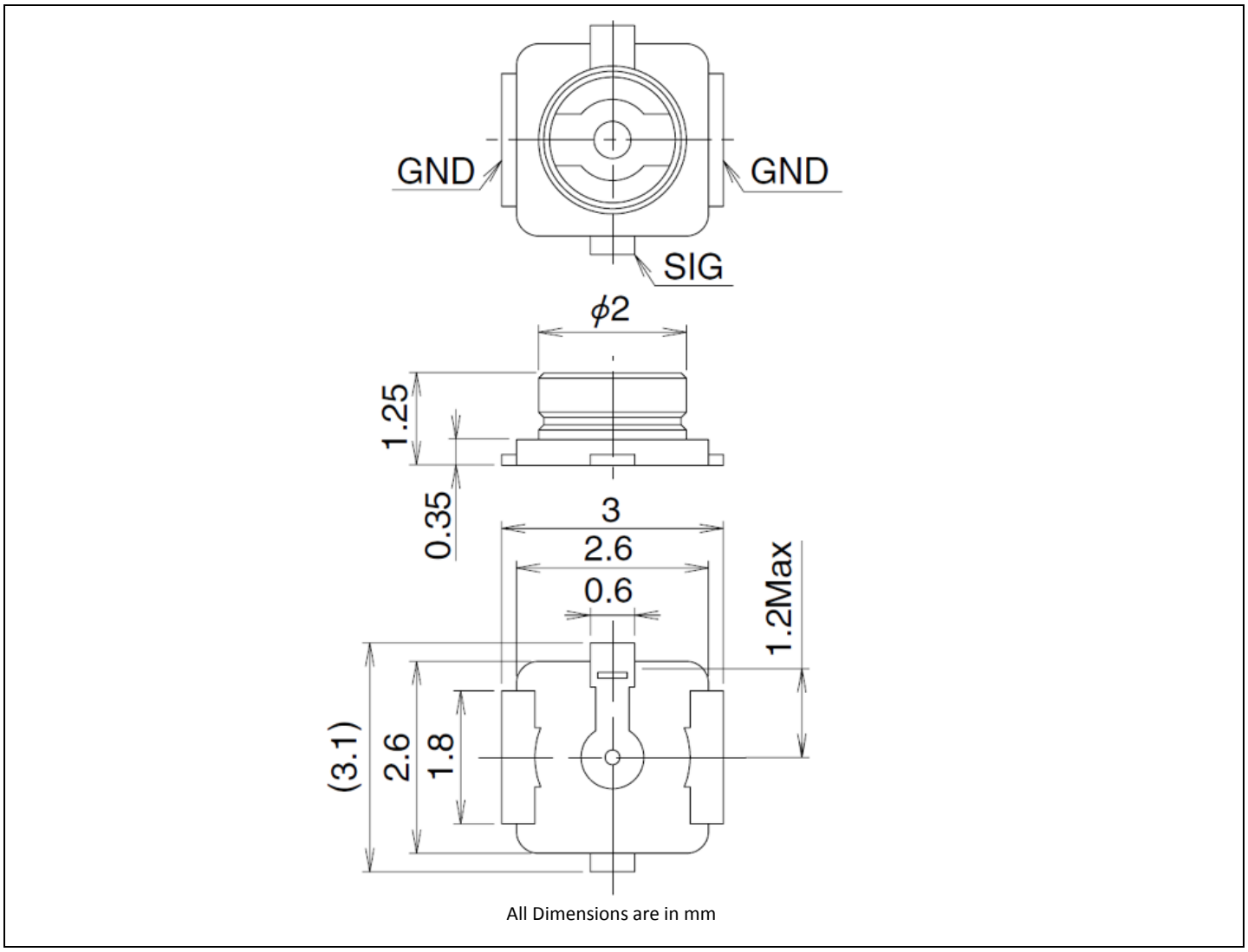


Figure 7. Hirose RF Connector for BT/Wi-Fi and ZigBee

The mechanical size of the Hirose connector (receptacle) is described in *Figure 7*. For suggestions on mating plug and more details on the connector, please contact Hirose Electric Co., LTD.

ARTIK 1020 Module Electrical Specifications

Absolute Maximum Ratings

The ratings given in this section are associated only with stress. It does not imply any functional operation of the device. Exposure to the absolute-maximum rated conditions for long duration affects the reliability of the device.

Table 24. Absolute Maximum Ratings

Con#:[Pin#]	Parameter	Symbol	Rating			Unit
			–	Min	Max	
–	Main battery supply	MAIN_BAT	–	-0.30	6.00	V
J1:[25,27,2,4,8,10,14,16,18,20,24, 26,28,30] J3:[15,17,19,21,23,25,27,29,31,33, 35,37,39,47,49,51,53,55,59,61,63, 65,71,73,75,77,18,20,22,24,26,28, 30,32,34,38,40,42,44,72,74,76,78, 80] J4:[1,3,5,7,9,11,13,15,17,19,21,45, 49,51,55,57,59,61,63,65,67,69,48, 50] J9:[17,19,25,27,29]	DC input/output voltage	VIN, VOUT	1.80 Input/output buffer	-0.5	2.50	V
			2.50 Input/output buffer	-0.5	3.60	V
			3.30 Input/output buffer	-0.5	3.80	V
	Input Output Current	I/O	–	±20		mA
J9: [6,8,10,12,14,16,18,20]	DC input/output voltage	–	1.80 Input/output buffer	-0.3	2.1	V
–	Storage Temperature	T_A	–	-40	125	°C

Note: Some pins on Connector J9 have a different behavior. If behavior is different it is explicitly noted in the table.

Table 25. Recommended Operating Conditions

Instances	Symbol	Min.	Typ.	Max.	Unit
Main Battery Supply	MAIN_BAT	3.13	3.80	4.80	V
Operating Temperature	T_A	-25	–	85	°C

POWER SUPPLY REQUIREMENTS

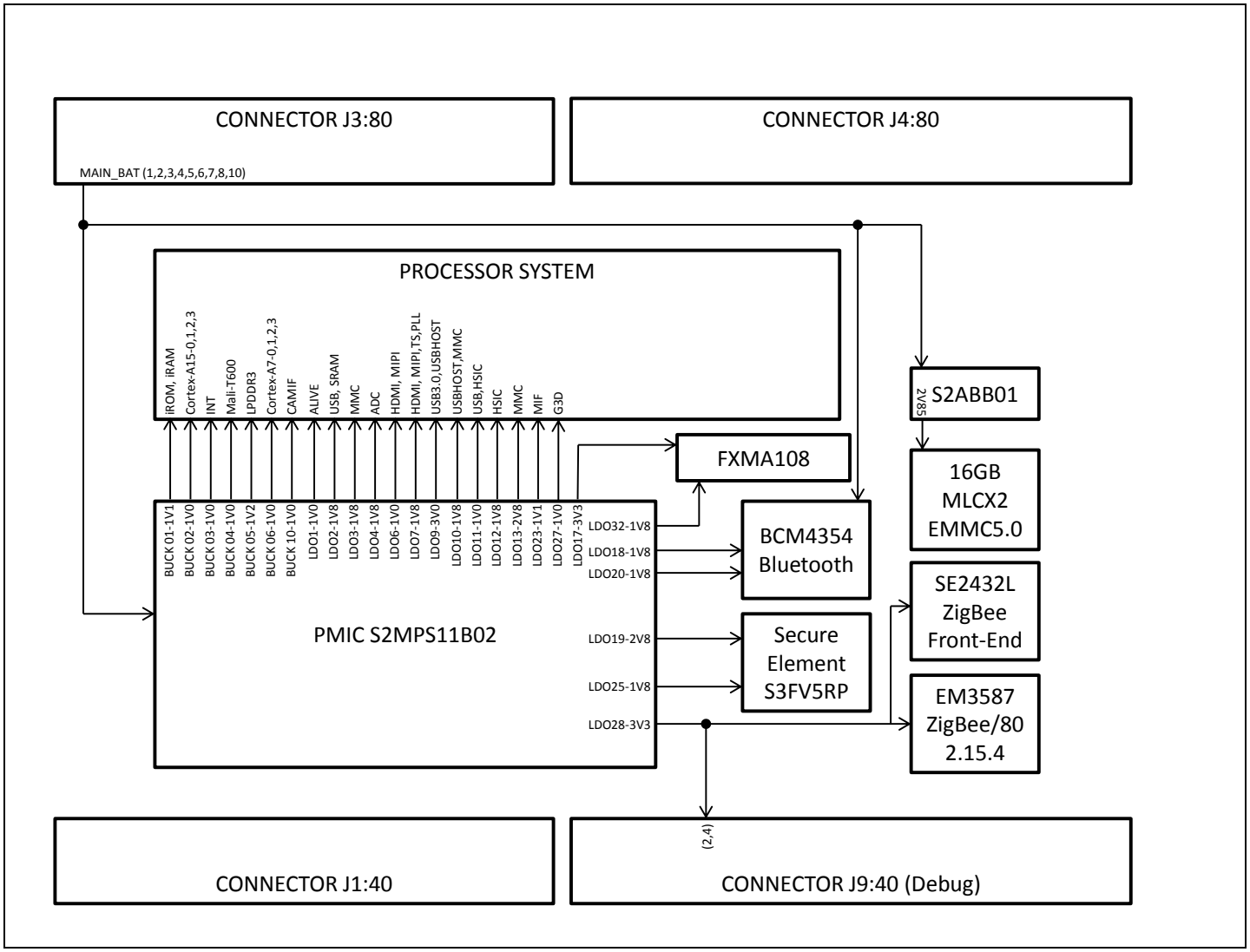


Figure 8. ARTIK 1020 Module Power Distribution

The power management of the ARTIK 1020 Module is controlled by the Samsung PMIC (S2MPS11B02). This PMIC contains 10 bucks and 38 LDO Regulators. See *Table 26* and *Table 27* for details on Voltage and Amperage ranges and how they are connected to the ARTIK 1020 Module.

Table 26. Buck Description and Default Setting

Buck Number	Pin	Powers	Current [A]	Range [V]	Step [mV]	Default [V]
1	PVDD_MIF_1V1	Processor System:[ROM, iRAM]	1.00	0.65-1.60	6.25	1.10
2	PVDD_ARM_1V0	Processor System:[Cortex®-A15-0,1,2,3]	7.00	0.65-1.60	6.25	1.00
3	PVDD_INT_1V0	Processor System:[INT]	2.50	0.65-1.60	6.25	1.00
4	PVDD_G3D_1V0	Processor System:[Mali™-T600]	4.00	0.65-1.60	6.25	1.00
5	PVDD_LPDDR3_1V2	Processor System:[LPDDR3]	3.00	0.65-2.0	6.25	1.20

Buck Number	Pin	Powers	Current [A]	Range [V]	Step [mV]	Default [V]
6	PVDD_KFC_1V0	Processor System:[Cortex®-A7-0,1,2,3]	1.00	0.65-1.60	6.25	1.00
7	VIN_LLDO_1V4	S2MPS11B02:[PMIC]	1.50	1.2-1.50	12.5	1.35
8	VIN_MLDO_2V0	S2MPS11B02:[PMIC]	2.50	1.8-2.10	12.5	2.00
9-boost	VIN_HLDO_3V5	S2MPS11B02:[PMIC]	1.50	3.00-3.75	25	3.40
10	VDD_CAM	Processor System:[CAMIF]	1.50	0.75-1.40	12.5	1.00

Table 27. LDO Settings with Default Values

LDO Number	Pin	Powers	Current [mA]	Range [V]	Step [mV]	Default [V]
LDO1(N)	PVDD_LDO1	Processor System:[Alive]	150	0.80-2.375	25	1.00
LDO2(P)	PVDD_LDO2	Processor System:[USB,SRAM]	450	0.8-3.95	50	1.80
LDO3(P)	PVDD_LDO3	Processor System:[MMC]	450	0.8-3.95	50	1.80
LDO4(P)	PVDD_LDO4	Processor System:[ADC]	150	0.8-3.95	50	1.80
LDO5(P)	PVDD_LDO5	NA	150	0.8-3.95	50	1.80
LDO6(N)	PVDD_LDO6	Processor System:[HDMI,MIPI]	300	0.8-2.375	25	1.00
LDO7(P)	PVDD_LDO7	Processor System:[TS,HDMI,MIPI,PLL]	300	0.8-3.95	50	1.80
LDO8(P)	PVDD_LDO8	NA	150	0.8-3.95	50	1.80
LDO9(P)	PVDD_LDO9	Processor System:[USB HOST, USB3.0]	150	0.8-3.95	50	3.00
LDO10(P)	PVDD_LDO10	Processor System:[USB HOST,MMC]	150	0.8-3.95	50	1.80
LDO11(N)	PVDD_LDO11	Processor System:[USB,HSIC]	300	0.8-2.375	25	1.00
LDO12(P)	PVDD_LDO12	Processor System:[HSIC]	150	0.8-3.95	50	1.80
LDO13(P)	PVDD_LDO13	Processor System:[MMC]	300	0.8-3.95	50	2.80
LDO14(P)	PVDD_LDO14	NA	150	0.8-3.95	50	3.00
LDO15(P)	PVDD_LDO15	NA	150	0.8-3.95	50	3.30
LDO16(P)	PVDD_LDO16	NA	150	0.8-3.95	50	2.20
LDO17(P)	PVDD_LDO17	FXMA108	300	0.8-3.95	50	3.30
LDO18(P)	PVDD_LDO18	BCM4354	450	0.8-3.95	50	1.80
LDO19(P)	PVDD_LDO19	S3FV5RP	300	0.8-3.95	50	2.80
LDO20(P)	PVDD_LDO20	BCM4354 (NC)	150	0.8-3.95	50	1.80
LDO21(P)	PVDD_LDO21	NA	150	0.8-3.95	50	1.80
LDO22(N)	PVDD_LDO22	NA	300	0.8-2.375	25	1.20
LDO23(N)	PVDD_LDO23	Processor System:[MIF]	150	0.8-2.375	25	1.10
LDO24(P)	PVDD_LDO24	NA	150	0.8-3.95	50	2.80
LDO25(P)	PVDD_LDO25	S3FV5RP	150	0.8-3.95	50	1.80
LDO26(P)	PVDD_LDO26	NA	150	0.8-3.95	50	3.00
LDO27(N)	PVDD_LDO27	Processor System:G3D	300	0.8-2.375	25	1.00
LDO28(P)	PVDD_LDO28	Connector J9:[2,4], EM3587, SE2432L	300	0.8-3.95	50	3.30
LDO29(P)	PVDD_LDO29	NA	300	0.8-3.95	50	1.80
LDO30(P)	PVDD_LDO30	NA	300	0.8-3.95	50	1.80
LDO31(P)	PVDD_LDO31	NA	150	0.8-3.95	50	1.80
LDO32(P)	PVDD_LDO32	FXMA108	300	0.8-3.95	50	1.80
LDO33(P)	PVDD_LDO33	NA	150	0.8-3.95	50	1.80

LDO Number	Pin	Powers	Current [mA]	Range [V]	Step [mV]	Default [V]
LDO1(N)	PVDD_LDO1	Processor System:[Alive]	150	0.80-2.375	25	1.00
LDO34(P)	PVDD_LDO34	NA	300	0.8-3.95	50	3.00
LDO35(N)	PVDD_LDO35	NA	300	0.8-2.375	25	1.20
LDO36(P)	PVDD_LDO36	NA	150	0.8-3.95	50	1.80
LDO37(P)	PVDD_LDO37	NA	150	0.8-3.95	50	1.80
LDO38(P)	PVDD_LDO38	NA	150	0.8-3.95	50	2.80

Table 28. AC/DC Characteristics of LDO28

LDO28, Connector J9:[2,4], MAIN_BAT=3.8V, T_A=25°C unless otherwise specified						
Characteristics	**Test Conditions**		**Min**	**Typ**	**Max**	**Unit**
Input voltage range (V_{INL})	–		2	V_{LDO}+0.2	MAIN_BAT	V
Under voltage lockout	Rising, 100mV hysteresis		–	1.60	1.70	V
Output voltage range	I_L=300mA programmable 50mV steps		0.80	–	3.95	V
Default output voltage	300mA@V_{INL}=V_{LDO}+0.2V		–	3.30	–	V
Maximum load current	Normal mode		300	–	–	mA
	Low power mode		5	–	–	mA
Output current limit	V_{OUT}=90% of V_{LDO}		330	510	900	mA
Minimum output bypass capacitance	–		1.5	2.2	–	µF
Ground Current	Battery supply current no load	Shutdown	–	<0.1	–	µA
		Normal regulation	–	21	30	
		Low power mode	–	3.5	6	
Output voltage accuracy	Normal mode V_{INL} = V_{LDO}+0.2V to MAIN_BAT, I_L=0.1mA-300mA		-3	–	3	%
	Low power mode V_{INL}=V_{LDO}+0.2V-MAIN_BAT, I_L = 0.1mA-5mA		-3	–	3	
Load Regulation	Normal mode V_{INL} = V_{LDO}+0.2V, I_L=0.1mA-300mA		–	0.1	–	%
	Low power mode V_{INL}=V_{LDO}+0.2V,I_L = 0.1mA-5mA		–	0.2	–	
Line Regulation	Normal mode V_{INL} = V_{LDO}+0.2V to MAIN_BAT, I_L=0.1mA		–	0.05	–	%/V
	Low power mode V_{INL}=V_{LDO}+0.2V-MAIN_BAT, I_L = 0.1mA		–	0.1	–	
Drop-out voltage	Normal mode V_{LDO}=3.3V, I_L=300mA		–	60	120	mV
	Normal mode V_{LDO}=1.8V, I_L=300mA		–	150	300	
	Low power mode V_{LDO}=3.3V, I_L=5mA		–	150	300	
Output load transient	Normal mode, V_{INL}=V_{LDO}+0.2V, I_L=3mA-300mA, and vice versa, t_r=t_f=10µs		–	60	90	mV
Output line transient	V_{INL}=V_{LDO}+0.2V to V_{LDO}+0.7V and vice versa, t_r=t_f=1µs, I_L=300mA		–	10	20	mV
Power Supply Rejection Ratio (PSRR)	f=1kHz to 4MHz, I_L=30mA, V_{INL}=V_{LDO}+0.2V+50mV_{pp}	1kHz	–	80	–	dB
		10kHz	–	65	–	
		100kHz	–	40	–	
		1MHz	–	35	–	
		4MHz	–	45	–	
Output Noise	f=10Hz-100kHz,C_L=2.2 µF, I_L=30mA	V_{LDO}=1.8V,V_{INL}=V_{LDO}+0.2V	–	60	–	µVrms
		V_{LDO}=3.3 V,V_{INL}=V_{LDO}+0.2V	–	80	–	
Soft Start	0 to 90% settling time		–	30	100	µs
Disable delay (t_{off})	After LDO is disabled; The LDO output voltage will discharge based on load current (I_L) and C_L		–	0.1	–	µs
Active discharge resistance	Output disabled		0.05	0.1	0.2	kΩ
Transition time from low power mode to normal mode (t_{ln}), and vice versa (t_{nl})	I_L=1mA		–	20	–	µs

LDO28, Connector J9:[2,4], MAIN_BAT=3.8V, T_A=25°C unless otherwise specified					
Characteristics	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Clamp Active Regulation Voltage	Clamp Active	V_{LDO}+3%	–	V_{LDO}+7%	V
Thermal shutdown	Tj rising	–	165	–	°C
	Tj falling	–	150	–	

Table 29. ESD Ratings

Symbol	Min.	Max.	Units
ESD Stress Voltage Human Body Model	–	1	kV
ESD stress voltage Charged Device Model	–	250	V

Table 30. Shock and Vibration Ratings

Shock and Vibration		Range
Shock	Operating	TBD
	Non Operating	TBD
Vibration	Operating	TBD
	Non Operating	TBD

DC Electrical Characteristics

I/O DC Electrical Characteristics

Table 31. I/O DC Electrical Characteristics Type A, B GPIO

TYPE A, B GPIO Con#:[Pin#]	Parameter		Condition	Min	Typ	Max	Units
J1:[25,27,2,4,8,10,14,16,18,20, 24,26,28,30] J3:[15,17,19,21,23,25,27,29,31, 33,35,37,39,47,49,51,53,55,59, 61,63,65,71,73,75,77,18,20,22, 24,26,28,30,32,34,38,40,42,44, 72,74,76,78,80] J4:[1,3,5,7,9,11,13,15,17,19,21, 45,49,51,55,57,59,61,63,65,67, 69,32,34,36,38,40,42,44,46,48, 50] J9:[17,19,25,27,29]	V_{tol}	V_{DD} power Off and On		–	–	3.60	V
	V_{ih}	High-level input voltage					
		CMOS interface		0.7xV_{DD}	–	V_{DD}+0.3	V
	V_{il}	Low-level input voltage					
		CMOS interface	V_{DD} = 1.8 V ±10 %	-0.3	–	0.3xV_{DD}	V
	ΔV	Hysteresis voltage	–	-0.15	–	–	V
	I_{ih}	High-level input current					µA
		Input buffer (V_{in}=V_{DD})	V_{DD} power On	-3	–	3	
			V_{DD} power Off and SNS = 0	-5	–	5	
		Input buffer with pull-down (V_{in}=V_{DD})	V_{DD} = 3.3V±10 %	20	45	80	
			V_{DD} = 1.8V±10 %	20	40	80	
	I_{il}	Low-level input current					µA
		Input buffer (V_{in}=V_{DD})	V_{DD} power On and Off	-3	–	3	
		Input buffer with pull-up (V_{in}=V_{DD})	V_{DD} = 3.3V±10%	-15	-40	-80	
			V_{DD} = 1.8V±10%	-15	-40	-80	
	V_{oh}	Output high voltage	Ioh= -1.8 mA, -3.6mA, -7.2mA, -10.8mA	0.8xV_{DD}	–	V_{DD}	V
	V_{ol}	Output low voltage	Ioh= -1.8mA, -3.6mA, -7.2mA, -10.8mA	0	–	0.2xV_{DD}	
	I_{oz}	Output Hi-Z current	-	-5	–	5	µA
	C_{IN}	Input capacitance	Any input and bi-directional buffers	–	–	5	pF

Note: V_{DD} = 1.80V for Type A I/O and V_{DD} = 2.80V for Type B I/O, T_j = – 40 to 85°C (junction temperature)

Table 32. I/O DC Electrical Characteristics ZIGBEE

ZIGBEE Con#:[Pin#]	Parameter	Test Condition	Min.	Typ.	Max.	Unit
J9:[6,8,10,12,14,18,20]	Low Schmitt switching threshold	V_{SWIL} Schmitt input threshold going from high to low	1.18	–	1.40	V
	High Schmitt switching threshold	V_{SWIH} Schmitt input threshold going from low to high	1.74	–	2.24	V
	Input current for logic 0	I_{IL}	–	–	-0.5	µA
	Input current for logic 1	I_{IH}	–	–	+0.5	µA
	Input pull-up resistor value	R_{IPU}	24	29	34	kΩ
	Input pull-down resistor value	R_{IPD}	24	29	34	kΩ
	Output voltage for logic 0	V_{OL} (I_{OL} = 4mA for standard pads, 8mA for high current pads)	0	–	0.50	V
	Output voltage for logic 1	V_{OH} (I_{OH} = 4mA for standard pads, 8mA for high current pads)	2.30	–	2.80	V
	Output source current (standard current pad)	I_{OHS}	–	–	4	mA
	Output sink current (standard current pad)	I_{OLS}	–	–	4	mA
	Output source current high current pad: Connector J9:8	I_{OHH}	–	–	8	mA
	Output sink current high current pad: Connector J9:8	$I_{OL}H$	–	–	8	mA
	Total output current (for I/O Pads)	$I_{OH} + I_{OL}$	–	–	40	mA

Table 33. I/O DC Electrical Characteristics ZIGBEE RESET

ZIGBEE Con#:[Pin#]	Parameter	Test Condition	Min.	Typ.	Max.	Unit
J9:[16]	Low Schmitt switching threshold	VSWIL Schmitt input threshold going from high to low	1.18	–	1.40	V
	High Schmitt switching threshold	VSWIH Schmitt input threshold going from low to high	1.74	–	2.24	V
	Input current for logic 0	I_{IL}	–	–	-0.5	µA
	Input current for logic 1	I_{IH}	–	–	+0.5	µA
	Input pull-up resistor value	R_{IPU} Pull-up value while the chip is not reset	24	29	34	kΩ
	Input pull-up resistor value	$R_{IPURESET}$ Pull-up value while the chip is reset	12	14.5	17	kΩ

Note: These conditions apply if external reset of EM3587 is needed. Usually reset of the EM3587 is performed by the Processor System.

Table 34. DC Electrical Characteristics PMIC

PMIC Con#:[Pin#]	Test Condition	Min	Typ	Max	Units
J1:[22]	High Schmitt switching threshold Logic input low level	–	–	0.4	V
	High Schmitt switching threshold Logic input high level	1.4	–	–	V
J4:[43]	Logic output from PMIC to Processor System input active low	–	–	0.2	V
	De-assert delay (PMIC Reset pin)	48	60	72	ms

USB DC Electrical Characteristics

Table 35. I/O DC Electrical Characteristics USB

USB Con#:[Pin#]	Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
J1:[31,33,37,39,34, 36,40] J3:[60,66,68] J4:[73,75,77,79]	High-level input voltage	V_{IH}	–	2.0	–	–	V
	Low-level input voltage	V_{IL}	–	–	–	0.8	
	High-level input current	I_{IH}	V_{in}=3.3V	-10	–	10	µA
	Low-level input current	I_{IL}	V_{in}=0V	-10	–	10	
	Static output high	V_{OH}	14.25kΩ to GND	2.8	–	3.6	V
	Static output low	V_{OL}	1.425kΩ to 3.6V	–	–	0.3	
	Valid level voltage	V_{BUS}	–	4.4	–	5.25	

Note: VBUS includes Xusb3VBUS0_0.

ADC DC Electrical Characteristics

Table 36. I/O DC Electrical Characteristics ADC

ADC Con#:[Pin#]	Characteristics	Symbol	Test Condition	Min	Typ	Max	Units
J3:[48,50,52,54,56,58]	Analog input range	Xadc0AIN0, Xadc0AIN1, Xadc0AIN2, Xadc0AIN5, Xadc0AIN6, Xadc0AIN7	–	0	–	1.80	V
	External input resistance	Xadc0AIN0, Xadc0AIN1, Xadc0AIN2, Xadc0AIN5, Xadc0AIN6, Xadc0AIN7	R_{lext}	–	50	–	Ω

Note: R_{lext} = Output resistance of the ADC driver = Output resistance of signal generator + series parasitic resistance between signal source and ADC input.

Table 37. I/O DC Electrical Characteristics ADC (Continued)

ADC Con#:[Pin#]	Characteristics	Test Condition		Min	Typ	Max	Units
J3:[48,50,52,54,56,58]	Resolution	–	–	–	12	–	bit
	Differential Non Linearity	1M Samples	PD = Low, HIGHF = High FCLK = 20 MHz, FSOC = 1 MHz FAIN = 10 kHz Ramp Wave	–	±1	±2	LSB
		50k Samples	PD = Low, HIGHF = Low FCLK = 1 MHz, FSOC = 50 kHz FAIN = 10 kHz Ramp Wave	–	±1	±2	LSB

ADC Con#:[Pin#]	Characteristics	Test Condition		Min	Typ	Max	Units
	Integral Non Linearity	1M Samples	PD = Low, HIGHF = High FCLK = 20 MHz, FSOC = 1 MHz FAIN = 10 kHz Ramp Wave	–	±2	±4	LSB
		50k Samples	PD = Low, HIGHF = Low FCLK = 1 MHz, FSOC = 50 kHz FAIN = 10 kHz Ramp Wave	–	±2	±4	LSB
	Offset voltage	Top and bottom offset voltage	PD = Low, HIGHF = Low FCLK = 1 MHz, FSOC = 50 kHz FAIN = 10 kHz Ramp Wave	–	±1	±2	LSB

Note: Typical values measured at AV_{DD} = 1.8V, AV_{SS} = 0.0V, T_A = 25 °C unless otherwise specified.

TYPE A I/O DRIVER STRENGTH

The driver strength for the various Type A I/O's operating at 1V8, that are available on Connectors J3, J4, J1, J9 (Debug) are given in *Table 38* and *Table 39*.

Table 38. I/O Driver Strength/Cell Delay Time

Type A Con#:[Pin#]	Input			Output PAD (Driving Capability)	Output PAD (Slew Rate)	CL=5pF	CL=10pF
	DS0	DS1	SR				
J1:[25,27,2,4,8,10,14,16,18,20,24,26,28,30] J3:[15,17,19,21,23,25,27,29,31,33,35,37,39,47,49,51,53,55,59,61,63,65,71,73,75,77,18,20,22,24,26,28,30,32,34,38,40,42,44,72,74,76,78,80] J4:[1,3,5,7,9,11,13,15,17,19,21,45,49,51,55,57,59,61,63,65,67,69,48,50] J9:[17,19,25,27,29]	0	0	0	2mA	Fast	1.9ns	2.5ns
	0	1	0	4mA	Fast	2.7ns	2.7ns
	1	0	0	8mA	Fast	1.1ns	1.2ns
	1	1	0	12mA	Fast	0.9ns	1.1ns
	0	0	1	2mA	Slow	2.7ns	3.3ns
	0	1	1	4mA	Slow	1.7ns	2.1ns
	1	0	1	8mA	Slow	1.4ns	1.6ns
	1	1	1	12mA	Slow	1.3ns	1.5ns

Table 39. Pull-up/down Resistor

Type A Con#:[Pin#]	V_{DD}=1.8V	Worst V_{DD}=1.65V T=125°C, Process=Slow	Worst V_{DD}=1.95V T=-40°C, Process=Fast
J1:[25,27,2,4,8,10,14,16,18,20,24,26,28,30] J3:[15,17,19,21,23,25,27,29,31,33,35,37,39,47,49,51,53,55,59,61,63,65,71,73,75,77,18,20,22,24,26,28,30,32,34,38,40,42,44,72,74,76,78,80] J4:[1,3,5,7,9,11,13,15,17,19,21,45,49,51,55,57,59,61,63,65,67,69,48,50] J9:[17,19,25,27,29]	Pull-up	45kΩ	13kΩ
	Pull-down	45kΩ	15kΩ

TYPE B I/O DRIVER STRENGTH

The driver strength for the various Type B I/O's operating at 3V3, that is available on Connector J9 (Debug) only are given in *Table 40* and *Table 41*.

Table 40. Type B I/O Driver Strength/Output Cell Delay Time

Type B Con#:[Pin#]	Input			Output PAD (Driving Capability)	CL=5pF	CL=10pF
	DS0	DS1	SR			
J4:[32,34,36,38,40,42,44,46]	0	0	0	x1	2.5ns	3.2ns
	0	1	0	x2	1.8ns	2.2ns
	1	0	0	x3	1.4ns	1.6ns
	1	1	0	x4	1.3ns	1.5ns
	0	0	1	x1	3.2ns	3.9ns
	0	1	1	x2	2.6ns	3.1ns
	1	0	1	x3	2.2ns	2.6ns
	1	1	1	x4	2.2ns	2.5ns

Table 41. Type B I/O Pull Up/Down Resistor

Type B Con#:[Pin#]	V_{DD}=3.3V±0.3V	Worst V_{DD}=3.00V T=125°C, Process=Slow	Typical V_{DD}=3.30V T=25°C, Process=Typical	Worst V_{DD}=3.60V T=-40°C, Process=Fast
J4:[32,34,36,38,40,42,44,46]	Pull-up	135kΩ	85kΩ	37kΩ
	Pull-down	165kΩ	80kΩ	44kΩ
Type B Con#:[Pin#]	**V_{DD}=2.5V±0.2V**	**Worst V_{DD}=2.30V T=125°C, Process=Slow**	**Typical V_{DD}=2.50V T=25°C, Process=Typical**	**Worst V_{DD}=2.70V T=-40°C, Process=Fast**
J4:[32,34,36,38,40,42,44,46]	Pull-up	140kΩ	68kΩ	25kΩ
	Pull-down	125kΩ	65kΩ	34kΩ
Type B Con#:[Pin#]	**V_{DD}=1.8V±0.15V**	**Worst V_{DD}=1.65V T=125°C, Process=Slow**	**Typical V_{DD}=1.80V T=25°C, Process=Typical**	**Worst V_{DD}=1.95V T=-40°C, Process=Fast**
J4:[32,34,36,38,40,42,44,46]	Pull-up	80kΩ	48kΩ	30kΩ
	Pull-down	80kΩ	48kΩ	30kΩ

DC Use Case Characteristics

Table 42. Use Case Characteristics

Use Case Description	Min	Typ	Max	Units
Image Tracking				mA
				V
Collision Avoidance				mA
				V
Object Detection				mA
				V
??				mA
				V

AC Electrical Characteristics

ADC AC Electrical Characteristics

Table 43. ADC AC Electrical Characteristics

ADC Con#:[Pin#]	Characteristics	Symbol	Test Condition	Min	Typ	Max	Units
J3:[48,50,52,54,56,58]	Main clock duty cycle ratio	–	–	45	50	55	%
	Analog input frequency	1M Samples	–	DC	–	100	kHz
		50k Samples	–	DC	–	5	kHz
	Normal operation current consumption	1M Samples	PD = Low, HIGHF = High FCLK = 20 MHz, FSOC = 1 MHz	–	500	–	µA
		50k Samples	PD = Low, HIGHF = Low FCLK = 1 MHz, FSOC = 50 kHz	–	100	–	µA
	Power down current	1M Samples	PD = High, HIGHF = High	–	0.2	–	µA
		50k Samples	PD = High, HIGHF = Low	–	0.2	–	µA
	Signal to Noise and Distortion Ratio (SNDR)	1M Samples	FCLK = 20MHz, FSOC = 1MHz FAIN = 100 kHz	54	60	–	dB
		50k Samples	FCLK = 1 MHz, FSOC = 50 kHz FAIN = 5 kHz	54	60	–	dB

SPI TIMING DIAGRAM

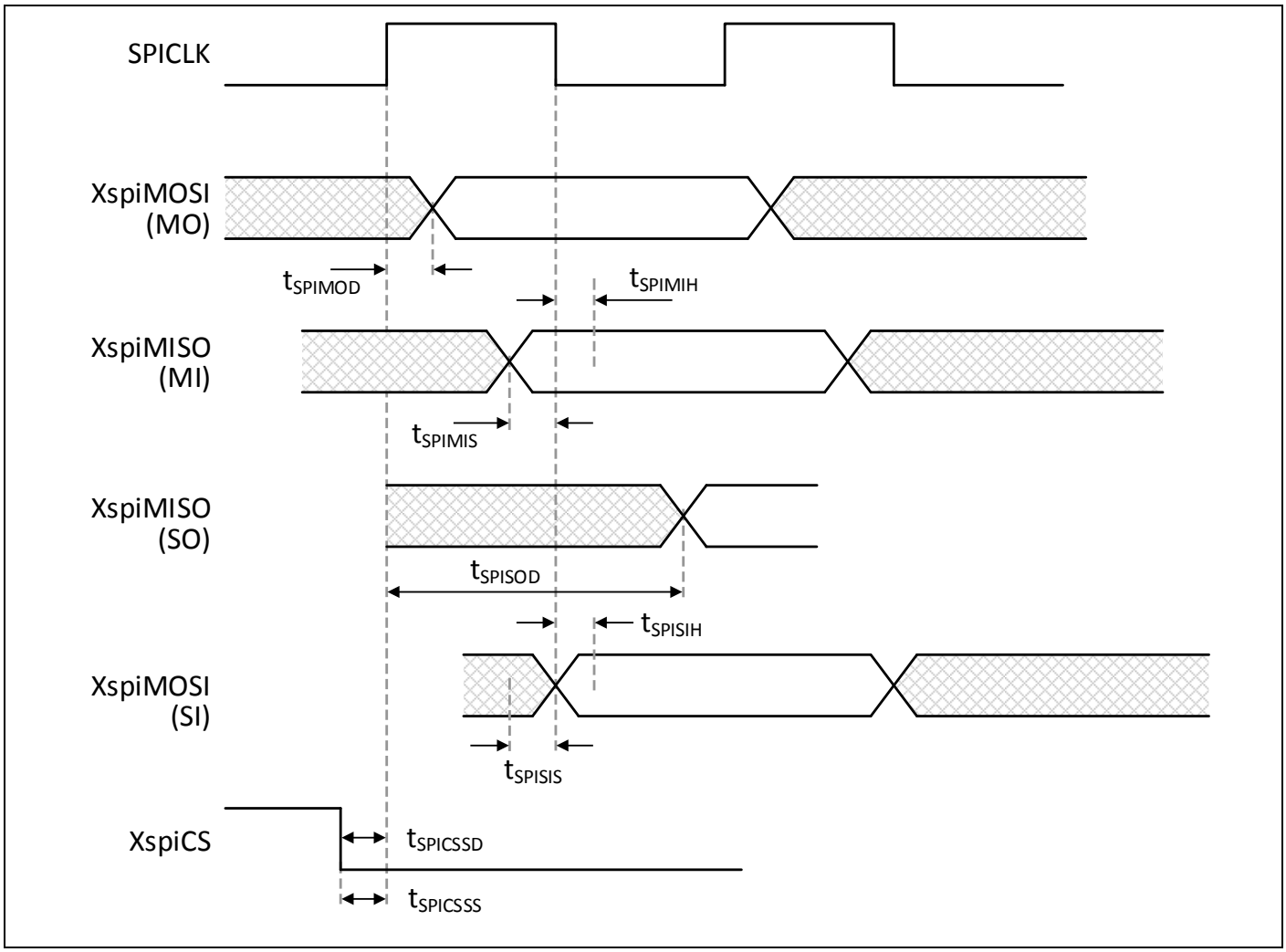


Figure 9. SPI Slave Mode Data Transfer Timing Diagram

SPI Timing Parameters

Table 44. SPI Timing Parameters

(V_{DDINT} = 1.0 V ± 5 %, TA = –25 to 85 °C, V_{DDext} = 1.8 V ± 10 %, load = 15 pF)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Ch 0	SPI MOSI Master Output Delay time	t_{SPIMOD}	–	–	5	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 00)	t_{SPIMIS}	12	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 01)		7	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 10)		2	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 11)		-3	–	–	
	SPI MISO Master Input Hold time	t_{SPIMIH}	5	–	–	
	SPI MOSI Slave Input Setup time	t_{SPISIS}	2	–	–	ns
	SPI MOSI Slave Input Hold time	t_{SPISIH}	5	–	–	
	SPI MISO Slave Output Delay time	t_{SPISOD}	–	–	17	
	SPI nSS Master Output Delay time	$t_{SPICSSD}$	7	–	–	
	SPI nSS Slave Input Setup time	$t_{SPICSSS}$	5	–	–	
Ch 1	SPI MOSI Master Output Delay time	t_{SPIMOD}	–	–	4	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 00)	t_{SPIMIS}	13	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 01)		8	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 10)		3	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 11)		-2	–	–	
	SPI MISO Master Input Hold time	t_{SPIMIH}	5	–	–	
	SPI MOSI Slave Input Setup time	t_{SPISIS}	3	–	–	
	SPI MOSI Slave Input Hold time	t_{SPISIH}	5	–	–	ns
	SPI MISO Slave Output Delay time	t_{SPISOD}	–	–	18	
	SPI nSS Master Output Delay time	$t_{SPICSSD}$	7	–	–	
	SPI nSS Slave Input Setup time	$t_{SPICSSS}$	5	–	–	

Note: SPICLKout = 50 MHz

- t_{SPIMIS},CH0 = 12 – (cycle period/4) x FB_CLK_SEL
- t_{SPIMIS},CH1 = 13 – (cycle period/4) x FB_CLK_SEL

I²C Timing Diagram

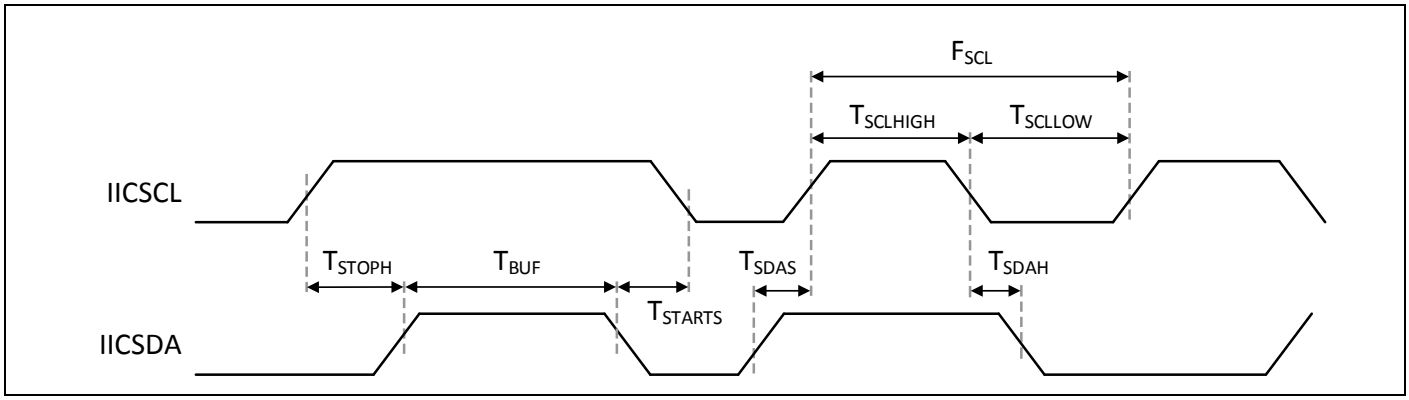


Figure 10. I²C Timing Diagram

I²C Timing Parameters

Table 45. I²C Timing Parameters

(V_{DDINT}, V_{DDarm} = 1.0 V ± 5 %, T_A = -25 to 85 °C, V_{DDext} = 1.8 V ± 10 %)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	F_{SCL}	–	–	std. 100 fast 400	kHz
SCL high level pulse width	$T_{SCLHIGH}$	std. 4.0 fast 0.6	–	–	µs
SCL low level pulse width	T_{SCLLOW}	std. 4.7 fast 1.3	–	–	
Bus free time between STOP and START	T_{BUF}	std 4.7 fast 1.3	–	–	
START hold time	T_{STARTS}	std. 4.0 fast 0.6	–	–	
SDA hold time	T_{SDAH}	std. 0 fast 0	–	–	
SDA setup time	T_{SDAS}	std. 250 fast 100	–	–	ns
STOP setup time	T_{STOPH}	std. 4.0 fast 0.6	–	–	µs

Note: std. refers to Standard Mode and fast refers to Fast Mode.

1. The I²C data hold time (t_{SDAH}) is minimum 0ns.
   (I²C data hold time is minimum 0ns for standard/fast bus mode I²C specification v2.1)
   Verify whether the data hold time of your I²C device is 0 ns.
2. The I²C controller supports I²C bus device (standard/fast bus mode). It does not support C bus devices.

eMMC Timing Diagram

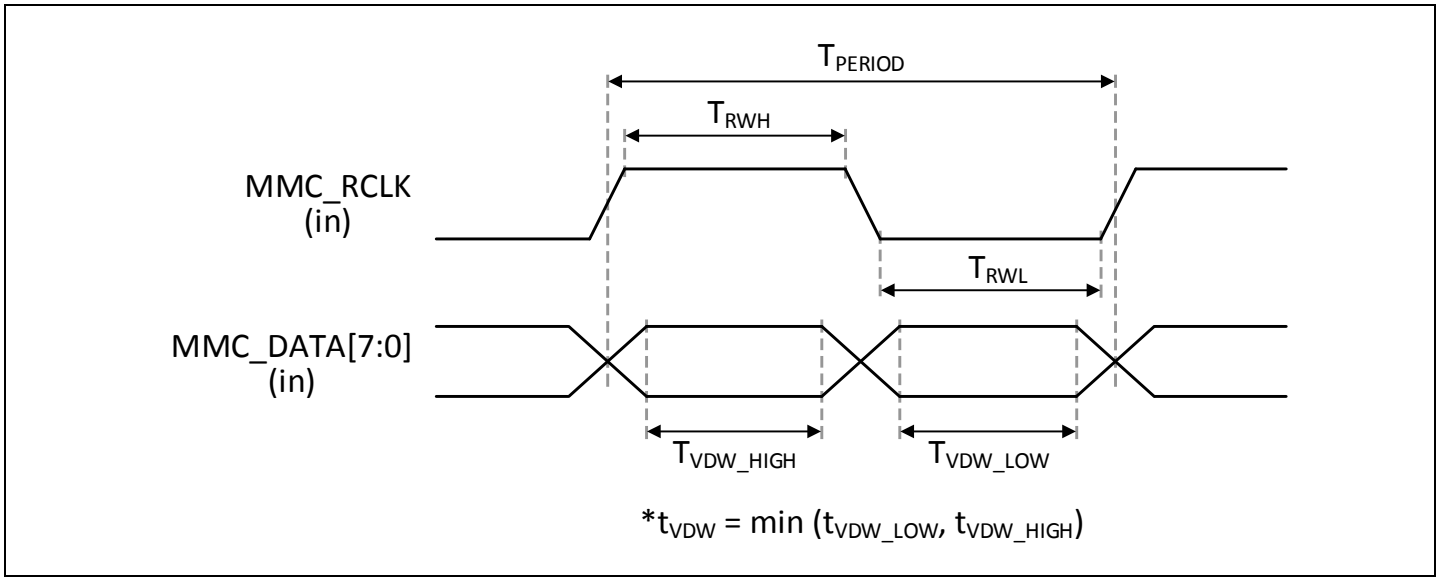


Figure 11. eMMC Timing Diagram

eMMC Timing Parameters

Table 46. eMMC Timing Parameters

Parameter	Symbol	Condition	Min	Max	Units
MMC_RCLK Cycle Time	T_{Period}	5	–	–	ns
MMC_RCLK High Time	T_{RWH}	1.5	–	–	
MMC_RCLK Low Time	T_{RWL}	1.5	–	–	
MMC Valid Data Window	T_{HSDDH}	1.0	–	–	

RF Electrical Characteristics

All performance numbers related to Wi-Fi, Bluetooth and ZigBee mentioned in this section are preliminary and likely to change once module characterization has taken place.

Wi-Fi WLAN 2.4GHz Receiver RF Specifications

Table 47. Wi-Fi WLAN 2.4GHz Receiver RF Specifications

Parameter	Conditions	Min	Typ.	Max	Unit
Minimum receiver sensitivity in 802.11b mode					
1Mbps	PER < 8%, Packet size = 1024 bytes	–	–	-80	dBm
2Mbps		–	–	-80	dBm
5.5Mbps		–	–	-76	dBm
11Mbps		–	–	-76	dBm
Minimum receiver sensitivity in 802.11g mode					
6Mbps	PER < 10%, Packet size= 1024 bytes	–	–	-82	dBm
9Mbps		–	–	-81	dBm
12Mbps		–	–	-79	dBm
18Mbps		–	–	-77	dBm
24Mbps		–	–	-74	dBm
36Mbps		–	–	-70	dBm
48Mbps		–	–	-66	dBm
54Mbps		–	–	-65	dBm
Minimum receiver sensitivity in 802.11n mode					
MCS 0	PER<10%, Packet size= 4096 bytes, GF, 800ns GI, Non-STBC	–	–	-82	dBm
MCS 1		–	–	-79	dBm
MCS 2		–	–	-77	dBm
MCS 3		–	–	-74	dBm
MCS 4		–	–	-70	dBm
MCS 5		–	–	-68	dBm
MCS 6		–	–	-65	dBm
MCS 7		–	–	-64	dBm
Minimum receiver sensitivity in 802.11ac mode (VHT20)					
MCS 0	PER<10%, Packet size= 4096 bytes, GF, 800ns GI, Non-STBC	–	–	-82	dBm
MCS 1		–	–	-79	dBm
MCS 2		–	–	-77	dBm
MCS 3		–	–	-74	dBm
MCS 4		–	–	-70	dBm
MCS 5		–	–	-66	dBm
MCS 6		–	–	-65	dBm
MCS 7		–	–	-64	dBm
MCS 8		–	–	-59	dBm
Maximum input level					
Maximum input signal level in 802.11b mode	PER < 8%	-10	–	–	dBm
Maximum input signal level in 802.11g mode	PER < 10%	-20	–	–	dBm

Parameter	Conditions	Min	Typ.	Max	Unit
Maximum input signal level in 802.11n mode	PER < 10%	-20	–	–	dBm
Maximum input signal level in 802.11ac mode	PER < 10%	-30	–	–	dBm

Wi-Fi WLAN 2.4GHz Transmitter RF Specifications

Table 48. Wi-Fi WLAN 2.4GHz Transmitter RF Specifications

Parameter	Conditions	Min	Typ.	Max	Unit
Linear output power					
Maximum output power in 802.11b mode	As specified in IEEE802.11	–	19	–	dBm
Maximum output power in 802.11g mode		–	16	–	dBm
Maximum output power in 802.11n mode	HT20	–	15	–	dBm
Maximum output power in 802.11ac mode	VHT20	–	15	–	dBm
Transmit spectrum mask					
Margin to 802.11b spectrum mask	Maximum output power	0	–	–	dBr
Margin to 802.11g spectrum mask		0	–	–	dBr
Margin to 802.11n spectrum mask		0	–	–	dBr
Transmit modulation accuracy in 802.11b mode					
1Mbps	As specified in IEEE 802.11b	–	–	35	%
2Mbps		–	–	35	%
5.5Mbps		–	–	35	%
11Mbps		–	–	35	%
Transmit modulation accuracy in 802.11g mode					
6Mbps	Mandatory	–	–	-5	dB
9Mbps	Optional	–	–	-8	dB
12Mbps	Mandatory	–	–	-10	dB
18Mbps	Optional	–	–	-13	dB
24Mbps	Mandatory	–	–	-16	dB
36Mbps	Optional	–	–	-19	dB
48Mbps	Optional	–	–	-22	dB
54Mbps	Optional	–	–	-25	dB
Transmit modulation accuracy in 802.11n mode					
MCS7	As specified in IEEE 802.11n	–	–	-27	dB
Transmit modulation accuracy in 802.11ac mode					
MCS8	VHT20	–	–	-30	dB
MCS9	VHT20	–	–	-32	dB
Transmit power-on and power-down ramp time in 802.11b mode					
Transmit power-on ramp time from 10% to 90% output power		–	–	2	µs
Transmit power-down ramp time from 90% to 10% output power		–	–	2	µs
Other spectral parameters					
Spurious emissions at the antenna port	30MHz ~ 1GHz BW=100kHz	–	–	-62	dBm
	1GHz~12.75GHz BW=1MHz	–	–	-47	dBm

BLUETOOTH RF SPECIFICATIONS

Table 49. Bluetooth RF Specifications

Parameter	Conditions	Min	Typ	Max	Unit
GFSK					
Output Power	Average Power	–	11	–	dBm
Frequency Range		2402	–	2480	MHz
Carrier Frequency Drift	DH1	-25	–	25	kHz
	DH3	-40	–	40	kHz
	DH5	-40	–	40	kHz
	Maximum Drift Rate	-20	–	20	kHz
Modulation	dF1 Avg	140	–	175	kHz
	dF2 Max	115	–	–	kHz
	dF1 Avg / dF2 Avg	80	–	–	%
Sensitivity (BER)	BER ≤0.1%	–	–	-70	dBm
Maximum Input Level	BER ≤0.1%	-20	–	–	dBm
EDR (DPSK)					
Relative Power	π/4-DQPSK	-4.0	–	1.0	dB
8DPSK		-4.0	–	–	dB
RMS DEVM	π/4-DQPSK	–	–	20.0	%
	8DPSK	–	–	13.0	%
Peak DEVM	π/4-DQPSK	–	–	35.0	%
	8DPSK	–	–	25.0	%
99% DEVM	π/4-DQPSK DEVM ≤ 0.30	99	–	–	%
	DEVM ≤ 0.20 8DPSK	99	–	–	%
EDR Sensitivity (BER)	π/4-DQPSK BER ≤ 0.01%	–	–	-70	dBm
	BER ≤ 0.01% 8DPSK	–	–	-70	dBm
EDR Maximum Input Level	π/4-DQPSK BER ≤ 0.1%	-20	–	–	dBm
	BER ≤ 0.1% 8 DPSK	-20	–	–	dBm
Low Energy					
Output Power	Output Power	-20	–	10	dBm
Operating Frequency	2402+K*2MHz (K=0~39)	2400	–	2483.5	MHz

ZigBee RF Receive Specifications

Receive measurements were collected with the ZigBee SoC Ceramic Balun Reference Design (Version A0) at 2440MHz. The typical number indicates one standard deviation above the mean, measured at room temperature (25°C). The Min and Max numbers were measured over process corners at room temperature.

Table 50. ZigBee RF Receive Specifications

Parameter	Test Condition	Min	Typ	Max	Unit
Frequency range		2400	–	2500	MHz
Sensitivity (boost mode)	1% PER, 20 byte packet defined by IEEE 802.15.4-2003;	–	-102	-96	dBm
Sensitivity	1% PER, 20 byte packet defined by IEEE 802.15.4-2003;	–	-100	-94	dBm
High-side adjacent channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	35	–	dB
Low-side adjacent channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	35	–	dB
2nd high-side adjacent channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	46	–	dB
2nd low-side adjacent channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	46	–	dB
High-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	39	–	dB
Low-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	47	–	dB
2nd high-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	49	–	dB
2nd low-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	49	–	dB
High-side adjacent channel rejection	CW interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	44	–	dB
Low-side adjacent channel rejection	CW interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	47	–	dB
2nd high-side adjacent channel rejection	CW interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	59	–	dB
2nd low-side adjacent channel rejection	CW interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	59	–	dB
Channel rejection for all other channels	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	40	–	dB
802.11g rejection centered at +12 MHz or -13 MHz	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	36	–	dB
Maximum input signal level for correct operation		0	–	–	dBm
Co-channel rejection	IEEE 802.15. 4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at -82 dBm	–	-6	–	dBc
Relative frequency error (50% greater than the 2x40 ppm required by IEEE 802.15.4-2003)		-120	–	+120	ppm

Parameter	Test Condition	Min	Typ	Max	Unit
Relative timing error (50% greater than the 2x40 ppm required by IEEE 802.15.4-2003)		-120	–	+120	ppm
Linear RSSI range	As defined by IEEE 802.15.4-2003	40	–	–	dB
RSSI Range		-90	–	-40	dB

ZigBee RF Transmit Specifications

Transmit measurements were collected with the Silicon Labs ZigBee SoC ceramic balun reference design (Version A0) at 2440 MHz. The typical number indicates one standard deviation below the mean, measured at room temperature of 25°C. The min and max numbers were measured over process corners at room temperature. In terms of impedance, this reference design presents a 3n3 inductor in parallel with a 100:50 balun to the RF pins.

Table 51. ZigBee RF Transmit Specifications

Parameter	Test Condition	Min	Typ	Max	Unit
Maximum output power (boost mode)	At highest boost mode power setting (+8)	–	8	–	dBm
Maximum output power	At highest normal mode power setting (+3)	1	5	–	dBm
Minimum output power	At lowest power setting	–	-55	–	dBm
Error vector magnitude (Offset-EVM)	As defined by IEEE 802.15.4-2003, which sets a 35% maximum	–	5	15	%
Carrier frequency error		-40	–	+40	ppm
PSD mask relative	3.5 MHz away	-20	–	–	dBm
PSD mask absolute	3.5 MHz away	-30	–	–	dBm

ARTIK 1020 Module Mechanical Specifications

The ARTIK 1020 Module supports three edge connectors and three RF connectors on a 39.0mmx29.0mm footprint. The size increases to 29.0mmx47.0mm if the additional debug connector is included. Refer to section *ARTIK 1020 Module Antenna Connections* for RF connector details. Layout and all mechanical dimensions mentioned in this section are preliminary and could change.

Table 52. Connectors J3, J4

	Connector Part Number	Number of pins	Pin pitch	Mating Part
Connector J3	Panasonic AXT480124	80	0.4mm	Panasonic AXT380124 (mated height 1.5mm) AXT380224 (mated height 2.5mm)
Connector J4				

Table 53. Connectors J1, J9

	Connector Part Number	Number of pins	Pin pitch	Mating Part
Connector J1	Panasonic AXT440124	40	0.4mm	Panasonic AXT340124 (mated height 1.5mm) AXT340224 (mated height 2.5mm)
Connector J9				

ARTIK 1020 Module Top View

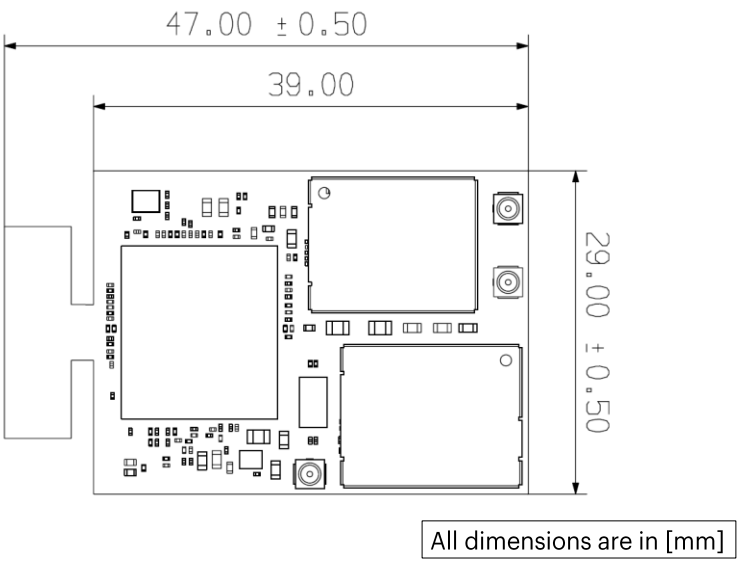


Figure 12. Top View ARTIK 1020 Module

ARTIK 1020 Module Bottom View

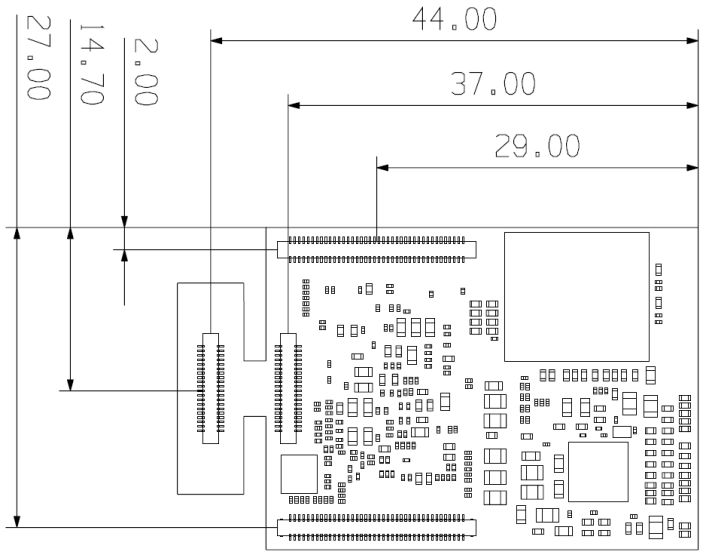


Figure 13. Bottom View ARTIK 1020 Module

ARTIK 1020 Module Side View

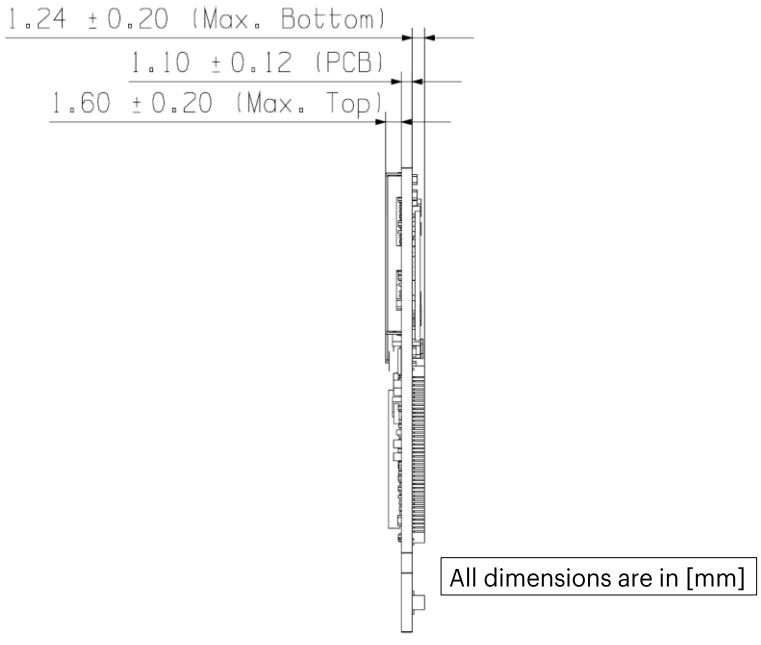


Figure 14. Side View ARTIK 1020 Module

ARTIK 1020 MODULE 3D VIEW

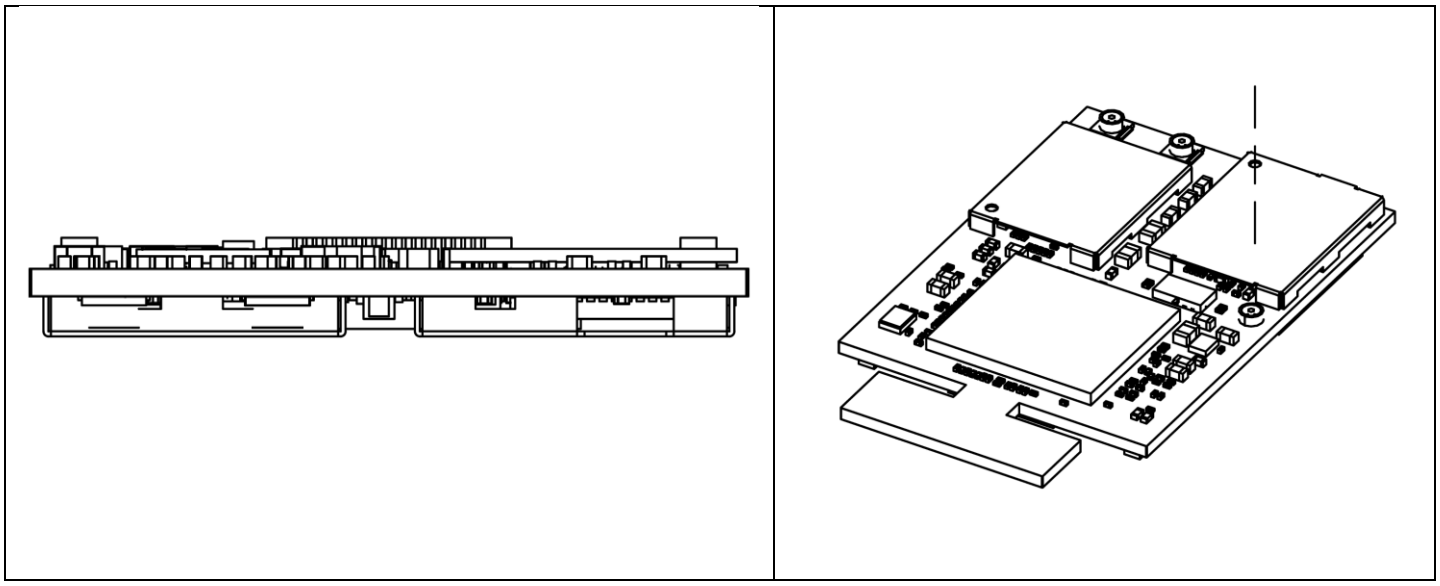


Figure 15. 3D View ARTIK 1020 Module

Ordering Information

For volume ordering of the evaluation kits, please contact a sales representative in your area or email sales@artik.io.

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