



AOD425

P-Channel Enhancement Mode Field Effect Transistor

General Description

The AOD425 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and ultra-low low gate charge with a 25V gate rating. This device is suitable for use as a load switch or in PWM applications. The device is ESD protected.

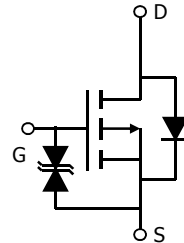
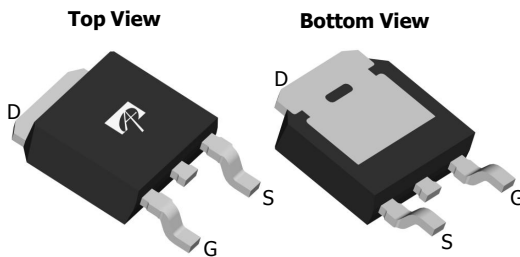
- RoHS Compliant
- Halogen Free*

Features

V_{DS} (V) = -30V
 I_D = -50A (V_{GS} = -10V)
 $R_{DS(ON)}$ < 17m Ω (V_{GS} = -10V)
 $R_{DS(ON)}$ < 35m Ω (V_{GS} = -5V)

ESD Protected!
100% Rg Tested!

**TO252
DPAK**



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

| Parameter | Symbol | Maximum | Units |
|--|----------------|-------------------------|------------------|
| Drain-Source Voltage | V_{DS} | -30 | V |
| Gate-Source Voltage | V_{GS} | ± 25 | V |
| Continuous Drain Current ^F | I_D | $T_C=25^\circ\text{C}$ | -50 |
| | | $T_C=100^\circ\text{C}$ | -36 |
| Pulsed Drain Current ^C | I_{DM} | -70 | A |
| Continuous Drain Current | I_{DSM} | $T_A=25^\circ\text{C}$ | -9 |
| | | $T_A=70^\circ\text{C}$ | -7 |
| Power Dissipation ^B | P_D | $T_C=25^\circ\text{C}$ | 71 |
| | | $T_C=100^\circ\text{C}$ | 36 |
| Power Dissipation ^A | P_{DSM} | $T_A=25^\circ\text{C}$ | 2.5 |
| | | $T_A=70^\circ\text{C}$ | 1.6 |
| Junction and Storage Temperature Range | T_J, T_{STG} | -55 to 175 | $^\circ\text{C}$ |

Thermal Characteristics

| Parameter | Symbol | Typ | Max | Units |
|--|-----------------|--------------|-----|---------------------------|
| Maximum Junction-to-Ambient ^A | $R_{\theta JA}$ | 16 | 20 | $^\circ\text{C}/\text{W}$ |
| Maximum Junction-to-Ambient ^A | | Steady-State | 41 | 50 |
| Maximum Junction-to-Case ^B | $R_{\theta JC}$ | 1.7 | 2.1 | $^\circ\text{C}/\text{W}$ |

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------------|---------------------------------------|--|------|--------------------|----------------|------------------|
| STATIC PARAMETERS | | | | | | |
| BV_{DSS} | Drain-Source Breakdown Voltage | $I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$ | -30 | | | V |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS}=-30\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$ | | | -1 -5 | μA |
| I_{GSS} | Gate-Body leakage current | $V_{DS}=0\text{V}$, $V_{GS}=\pm 25\text{V}$ | | | ± 10 | μA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$ | -1.5 | -2.45 | -3.5 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}=-10\text{V}$, $V_{DS}=-5\text{V}$ | -70 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}=-10\text{V}$, $I_D=-20\text{A}$ $T_J=125^\circ\text{C}$ $V_{GS}=-5\text{V}$, $I_D=-20\text{A}$ | | 13.5 18.5 27 | 17 24 35 | $\text{m}\Omega$ |
| g_{FS} | Forward Transconductance | $V_{DS}=-5\text{V}$, $I_D=-20\text{A}$ | | 27 | | S |
| V_{SD} | Diode Forward Voltage | $I_S=-1\text{A}$, $V_{GS}=0\text{V}$ | | -0.72 | -1 | V |
| I_S | Maximum Body-Diode Continuous Current | | | | -50 | A |
| DYNAMIC PARAMETERS | | | | | | |
| C_{iss} | Input Capacitance | $V_{GS}=0\text{V}$, $V_{DS}=-15\text{V}$, $f=1\text{MHz}$ | | 1760 | 2200 | pF |
| C_{oss} | Output Capacitance | | | 360 | | pF |
| C_{rss} | Reverse Transfer Capacitance | | | 255 | | pF |
| R_g | Gate resistance | $V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$ | | 6.4 | 8 | Ω |
| SWITCHING PARAMETERS | | | | | | |
| $Q_g(10\text{V})$ | Total Gate Charge | $V_{GS}=-10\text{V}$, $V_{DS}=-15\text{V}$, $I_D=-20\text{A}$ | | 30 | 38 | nC |
| $Q_g(4.5\text{V})$ | Total Gate Charge | | | 11 | | nC |
| Q_{gs} | Gate Source Charge | | | 7 | | nC |
| Q_{gd} | Gate Drain Charge | | | 8 | | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}=-10\text{V}$, $V_{DS}=-15\text{V}$, $R_L=0.75\Omega$, $R_{GEN}=3\Omega$ | | 11.5 | | ns |
| t_r | Turn-On Rise Time | | | 8 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 35 | | ns |
| t_f | Turn-Off Fall Time | | | 18.5 | | ns |
| t_{rr} | Body Diode Reverse Recovery Time | $I_F=-20\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$ | | 24 | 30 | ns |
| Q_{rr} | Body Diode Reverse Recovery Charge | $I_F=-20\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$ | | 16 | | nC |

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}=175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=175^\circ\text{C}$.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 us pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=175^\circ\text{C}$. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$.

*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

Rev3: May. 2010

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

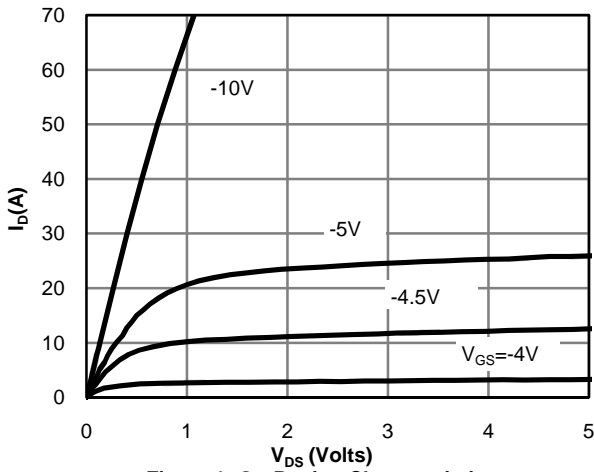


Figure 1: On-Region Characteristics

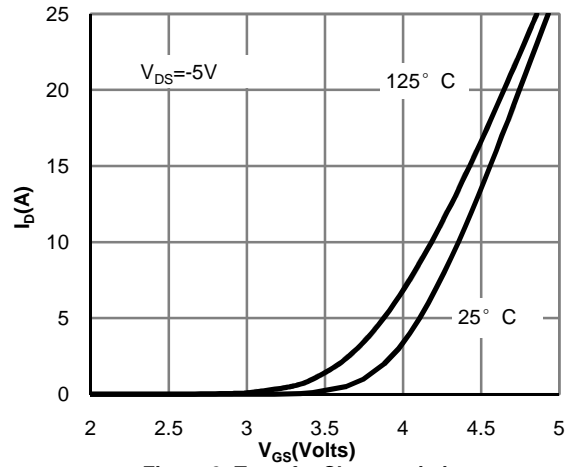


Figure 2: Transfer Characteristics

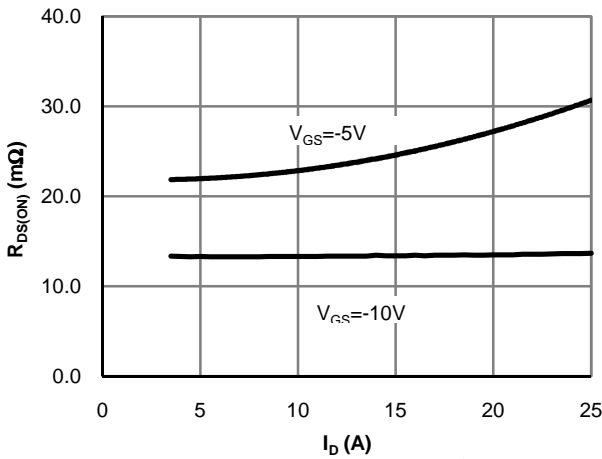


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

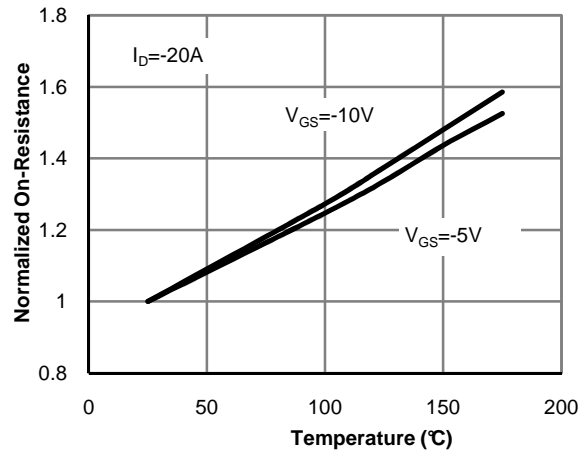


Figure 4: On-Resistance vs. Junction Temperature

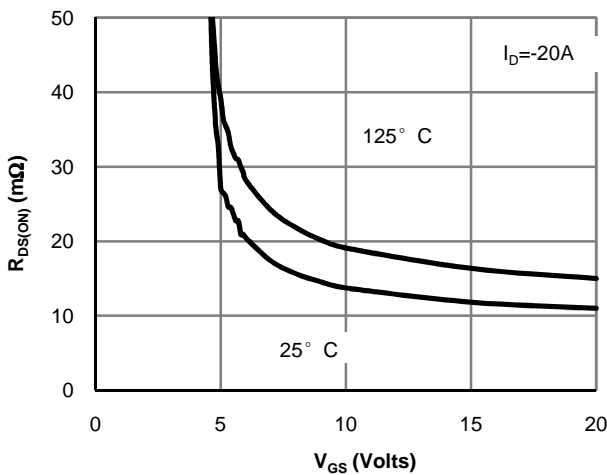


Figure 5: On-Resistance vs. Gate-Source Voltage

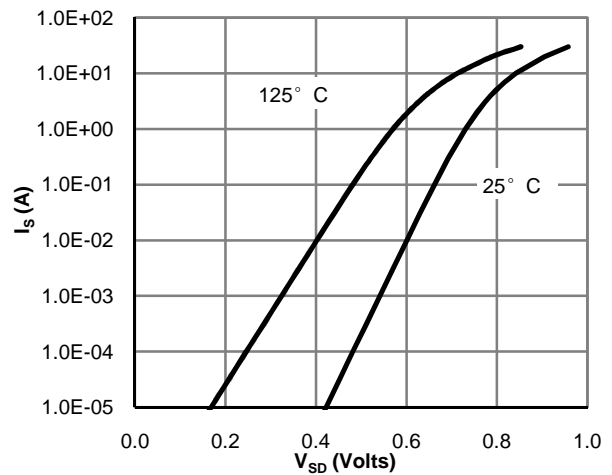


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

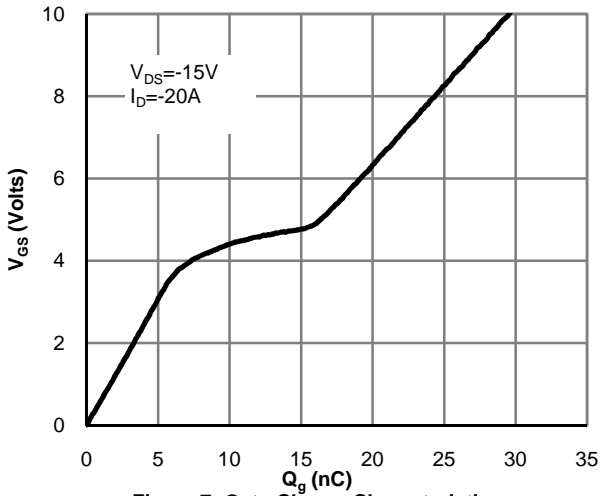


Figure 7: Gate-Charge Characteristics

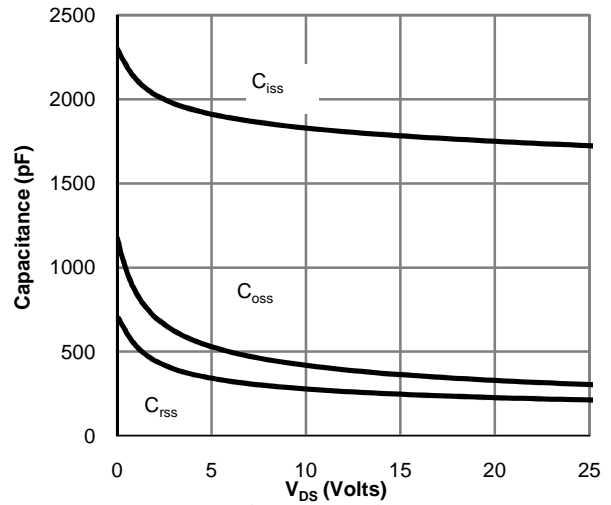


Figure 8: Capacitance Characteristics

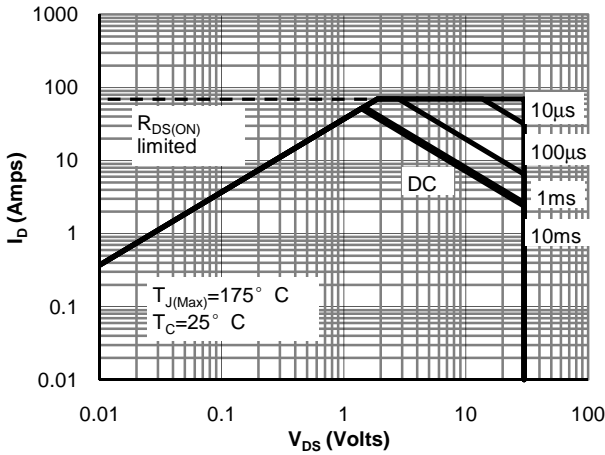


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

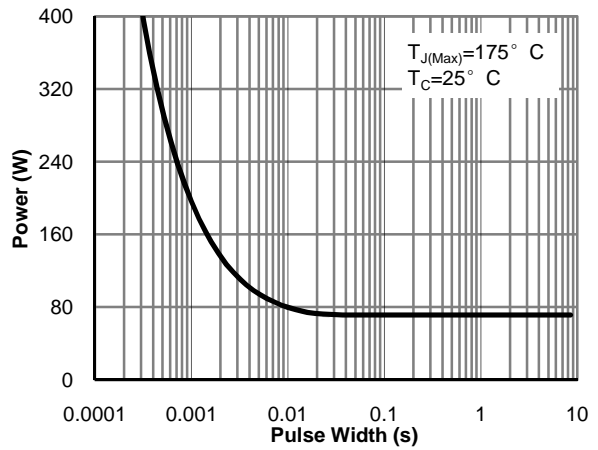


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

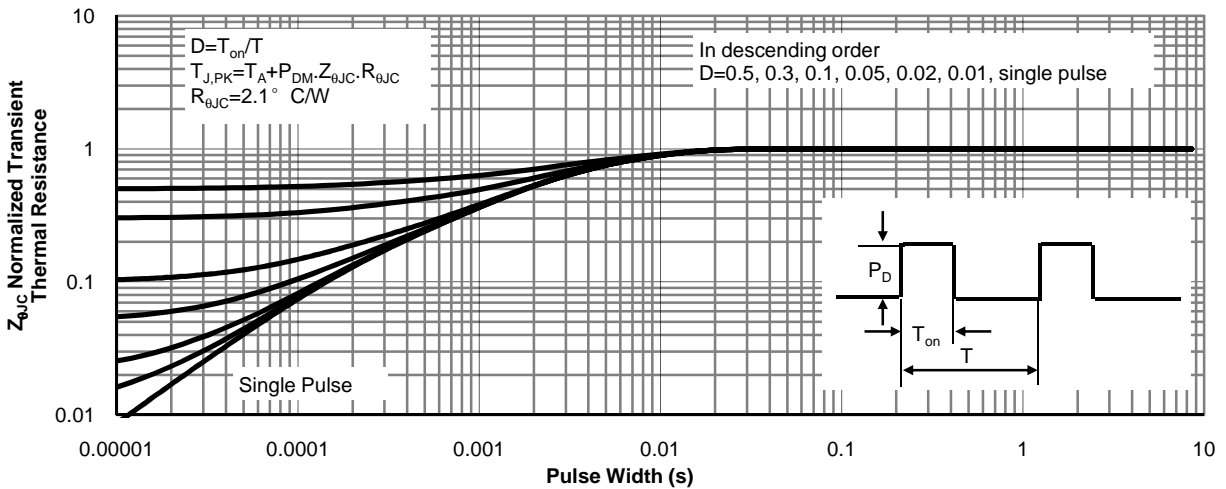


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

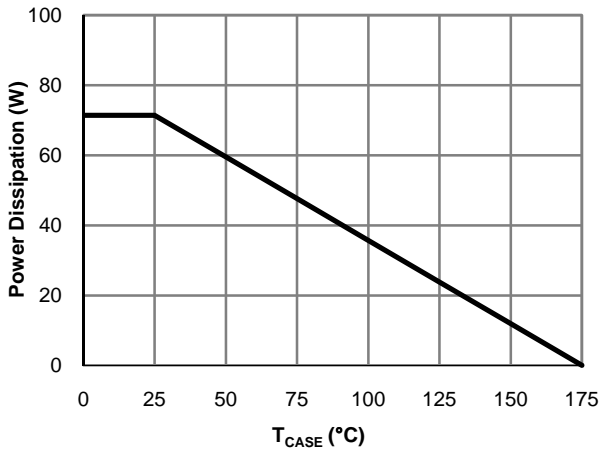


Figure 13: Power De-rating (Note B)

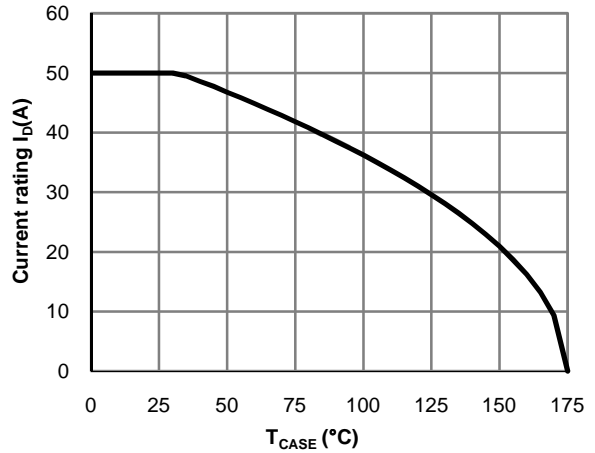


Figure 14: Current De-rating (Note B)

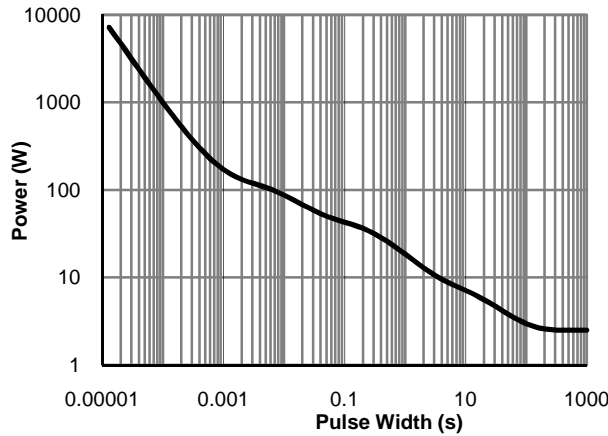


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

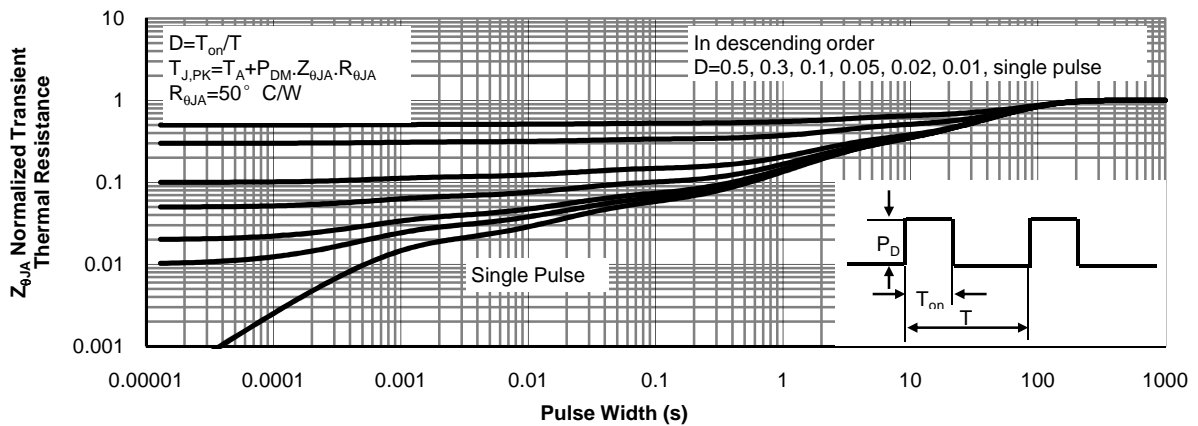
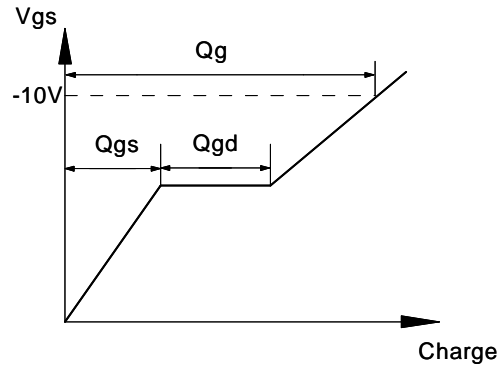
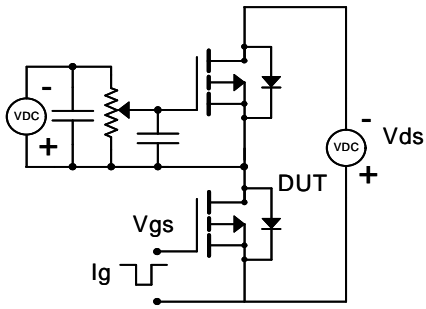
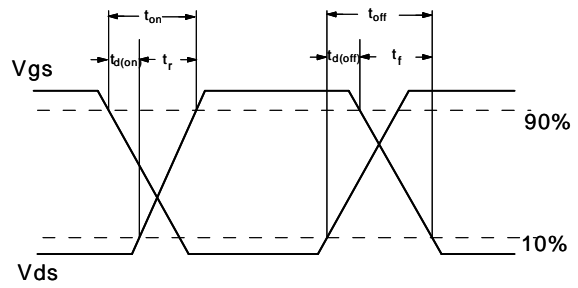
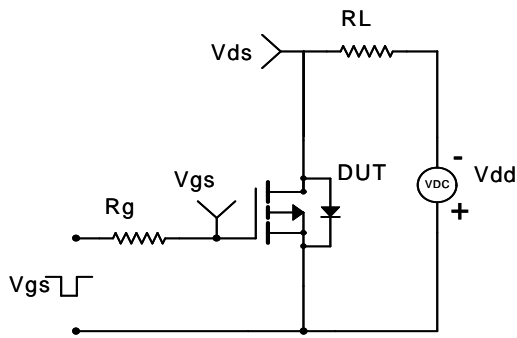


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

